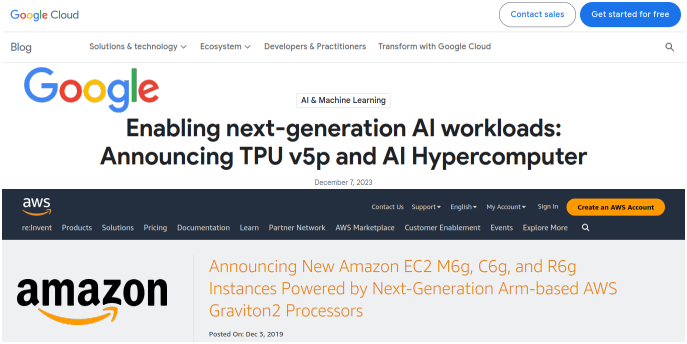
Automating the Design of Programmable Interconnect for Reconfigurable Architectures

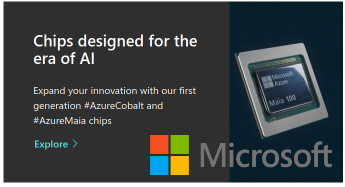
Stefan Nikolić

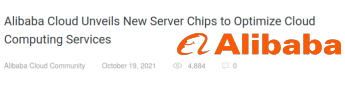
EPFL, 14.12.2023

École Polytechnique Fédérale de Lausanne

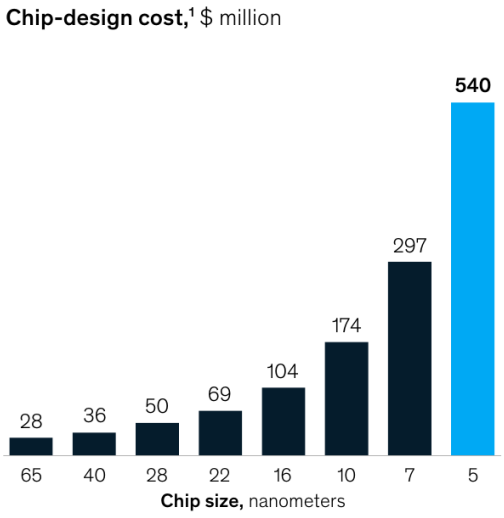
Custom Hardware Is Our Reality







But What If We Don’t Have $0.5B?



Source: H. Bauer et al. Semiconductor design and manufacturing: Achieving leading-edge capabilities. McKinsey & Company, 2020

It’s All Like a Movie

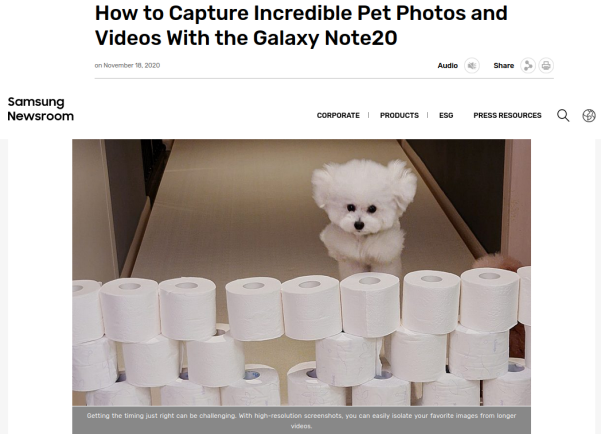
Professional cinematography is expensive

Sven Nykvist and Andrei Tarkovsky, 1986

Average feature film budget: $100-150 million
(https://www.nfi.edu/how-much-does-it-cost-to-make-a-movie/)

It’s All Like a Movie

But a DIY shot of your dog playing might be more valuable



FPGA: The Cell-Phone Camera of Custom Hardware

AMD
XILINX

ALTERA
now part of Intel

IEEE Spectrum FOR THE TECHNOLOGY INSIDER

Type to search

ARTICLE | HISTORY OF TECHNOLOGY

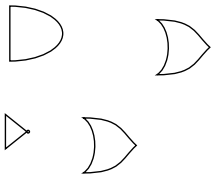
Chip Hall of Fame: Xilinx XC2064 FPGA ›

Hardware that can transform itself on command has proven incredibly useful

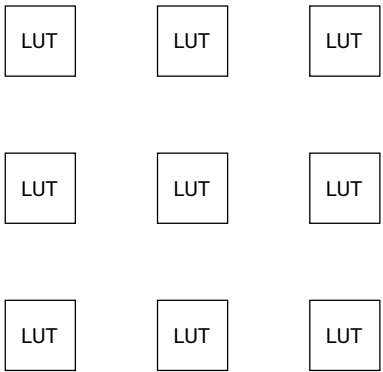
BY IEEE SPECTRUM | 30 JUN 2017 | 1 MIN READ

FPGA: The Cell-Phone Camera of Custom Hardware

fixed gates



reconfigurable generic gates

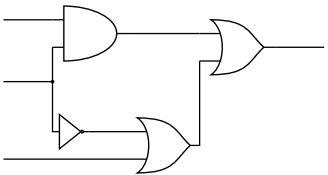


ASIC

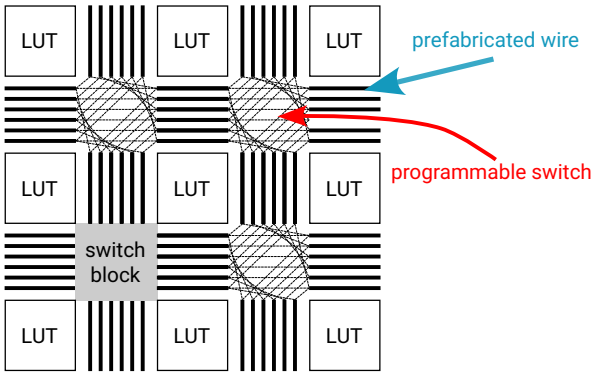
FPGA

FPGA: The Cell-Phone Camera of Custom Hardware

fixed interconnect



programmable interconnect



ASIC

FPGA

Cameras Got Better Over Time

Pentax *ist D
Year: 2003
Price (inflation adjusted): $2500 (body only)

Google Pixel 8
Year: 2023
Price: $700

And So Did FPGAs

Three Ages of FPGAs: A Retrospective on the First Thirty Years of FPGA Technology

This paper reflects on how Moore's Law has driven the design of FPGAs through three epochs: the age of invention, the age of expansion, and the age of accumulation.

By Stephen M. (Steve) Trimberger, *Fellow IEEE*

nology in the early 1990s. As a result, FPGAs began the Age of Expansion lagging the process introduction curve. In the 1990s, they became process leaders as the foundries realized the value of using the FPGA as a process-driver application. Foundries were able to build SRAM FPGAs as soon as they were able to yield transistors and wires in a new technology. FPGA vendors sold their huge devices while foundries refined their processes. Each new generation of silicon

For two decades, FPGAs were fabrication technology drivers, first to profit from Moore's law

The “Let Moore Do It” Era of Programmable Interconnect Design

Architectural Enhancements in Stratix V™

David Lewis*, David Cashman*, Mark Chan, Jeffery Chromczak*, Gary Lai, Andy Lee, Tim Vanderhoek*, Haiming Yu
Altera Corporation, 101 Innovation Drive, San Jose, CA, 95134
(*) Altera Corporation, 150 Bloor St W., Suite 400, Toronto, Ont., Canada M5S 2X9
{dlewis,dcashman,mchan,jchrmomcz,glai,alee,tvanderh,hyu}@altera.com

Although relatively small, the modularity results in a desire to accommodate a moderate increase in routing demand with adjustments to wire length, rather than the coarser quantization of increasing columns of routing multiplexers. Consequently rather than completely re-architect the routing, we explored minor variations that could keep pace with the increase in routing demand as well as obtain performance improvement.

ALTERA
now part of Intel

Rule 1: Minimize changes

Computer History Museum

AMD
XILINX

Rule 2: Rely on intuition

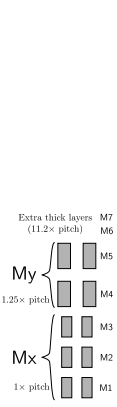
Oral History of Steve Trimberger

Trimberger: So we just flew through that, and it actually made a lot of really good decisions because we had a lot of people with expertise at that point, which we didn't have five years earlier because there just wasn't that much expertise in the FPGA business.

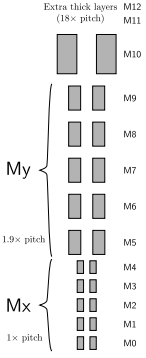
Interviewed by:
Doug Fairbairn
Jesse Jenkins

The End of an Era

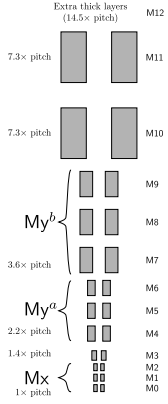
Wire scaling has become problematic



16nm

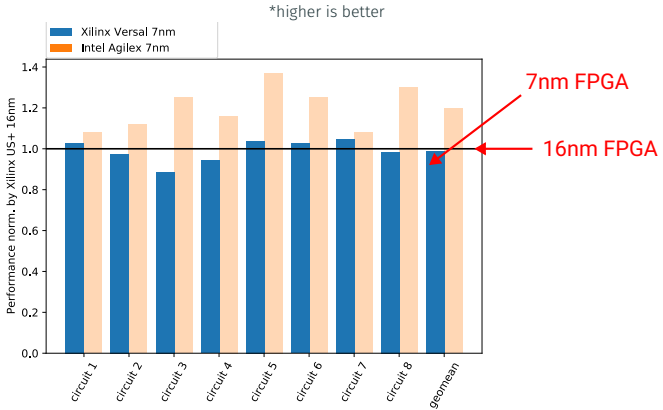


7nm



3nm

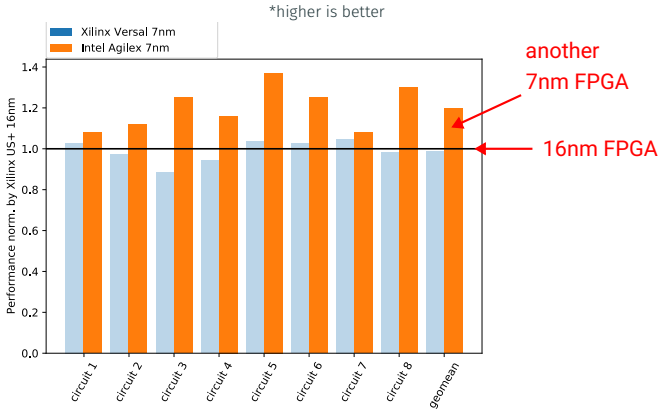
The End of an Era



Source: Z. Weng and K. Tondehal. Performance Advantages on OpenCores with Intel Agilex® 7 FPGAs. Intel White Paper 787066, 2023

Scaling no longer makes FPGAs faster

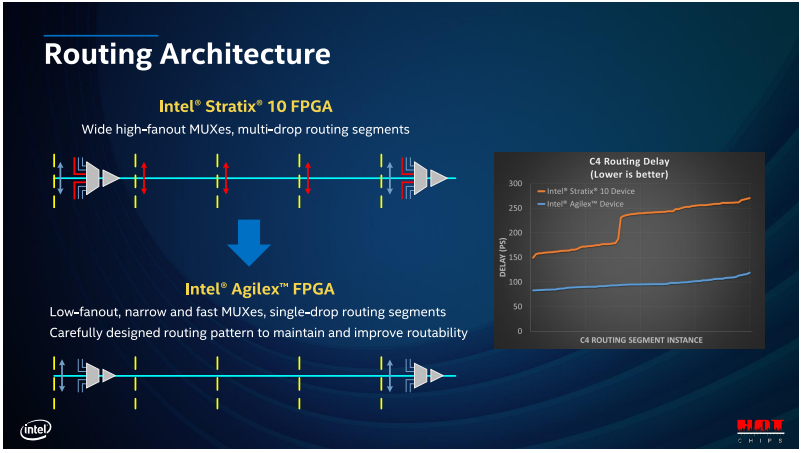
The End of an Era



Source: Z. Weng and K. Tondehal. Performance Advantages on OpenCores with Intel Agilex® 7 FPGAs. Intel White Paper 787066, 2023

But how did Agilex get it better?

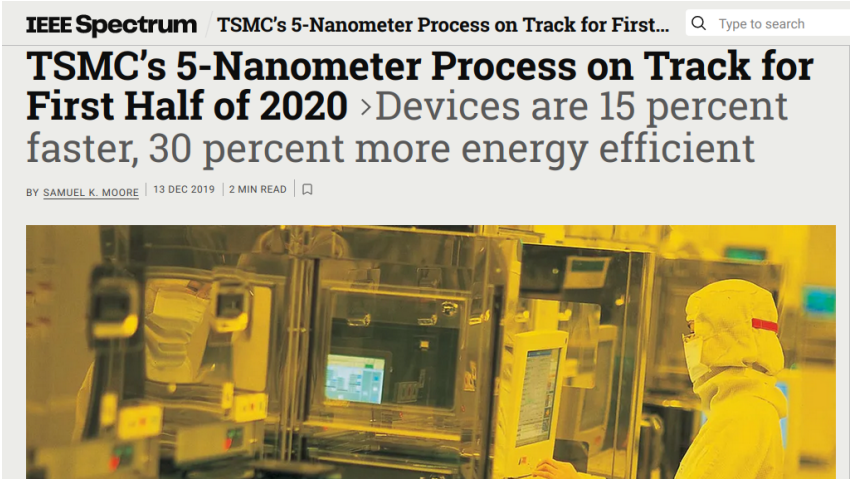
How Did Agilex Get It Better?



Source: I. Ganusov, M. Iyer, N. Cheng, A. Meisler. Agilex™ Generation of Intel® FPGAs. Hot Chips 2020

By drastically redesigning the programmable interconnect architecture

And What Was the Cost?



FPGAs now lag behind the latest technology by two full nodes

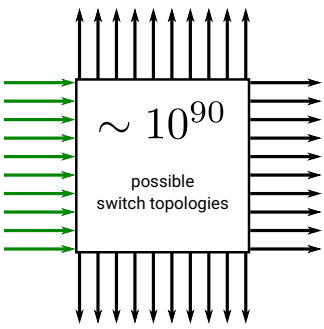
Can’t We Design Programmable Interconnect More Quickly?

Yes, by design automation

What Makes Programmable Interconnect Design Automation Difficult?

1. Critical paths unknown at fabrication time (before each user circuit is programmed)
   $\Longrightarrow$ need to optimize for the typical case
   $\Longrightarrow$ inherently empirical

2. Huge design spaces

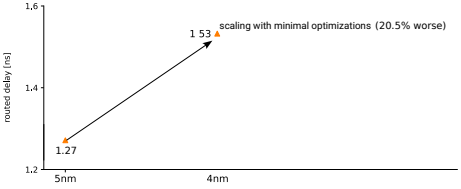


So can we automate
programmable interconnect design?

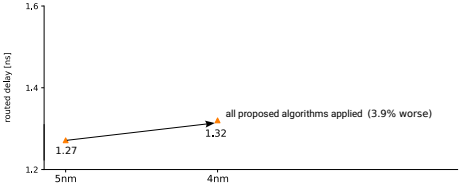
Yes We Can!

This thesis introduced several new algorithms that showed this possible.

*lower is better



Moving to a future technology node without this thesis

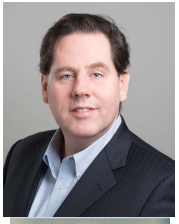
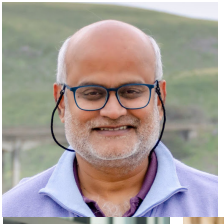


Moving to a future technology node with this thesis

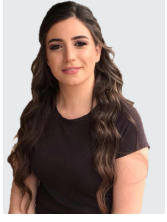
advisor thesis committee

Prof. Dr. Paolo Ienne | Prof. Dr. Vaughn Betz | Dr. Dinesh Gaitonde | Prof. Dr. Christoph Studer | Prof. Dr. Giovanni De Micheli

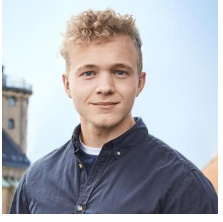
advisor

collaborators







Dr. Grace Zgheib | Prof. Dr. Francky Catthoor | Dr. Zsolt Tőkei | Dr. Mirjana Stojilović | Mr. Morten B. Petersen

THANK YOU