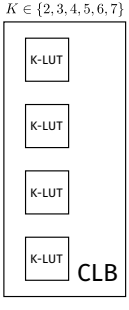
Turning PathFinder Upside-Down:
Exploring FPGA Switch-Blocks by Negotiating Switch Presence

Stefan Nikolić and Paolo Ienne

FPL'21, Dresden, 02.09.2021

École Polytechnique Fédérale de Lausanne

How Do We Explore FPGA Architecture?



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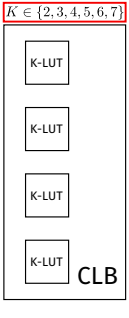

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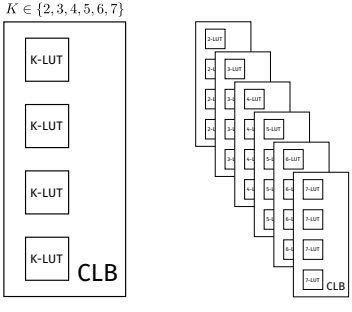

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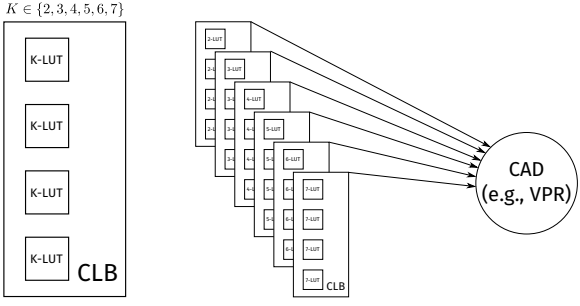

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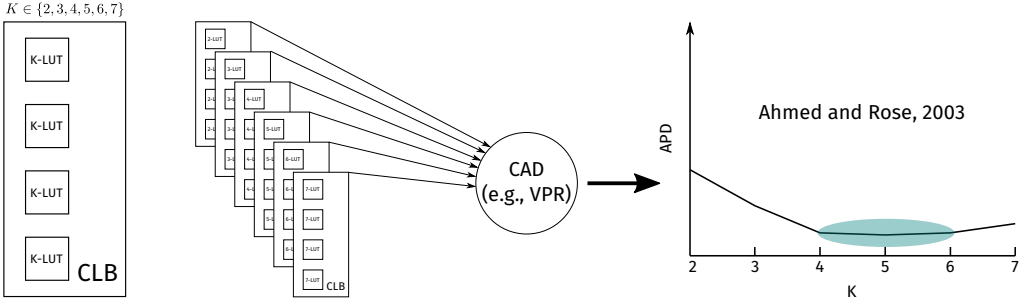

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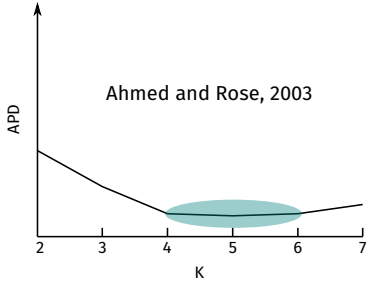

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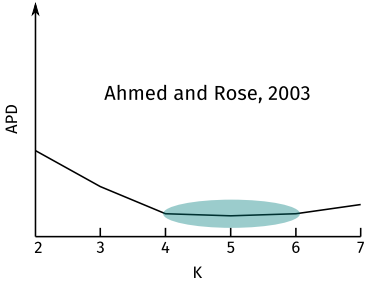

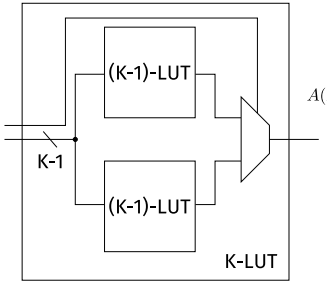

$A(K\text{-LUT}) > 2 \times A((K-1)\text{-LUT})$

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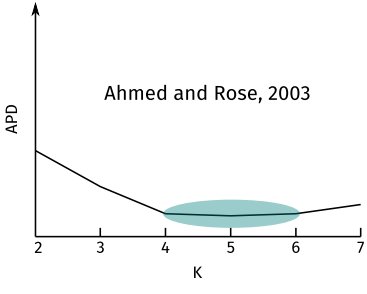

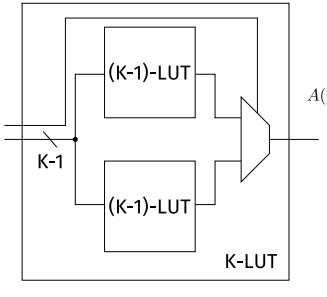

$A(K\text{-LUT}) > 2 \times A((K-1)\text{-LUT})$

Similar approach applicable to cluster size, channel composition, etc.

How Do We Explore FPGA Architecture?

What about Switch-Block Patterns?

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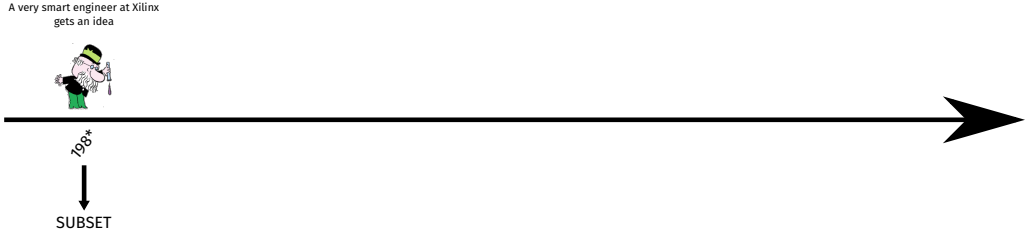

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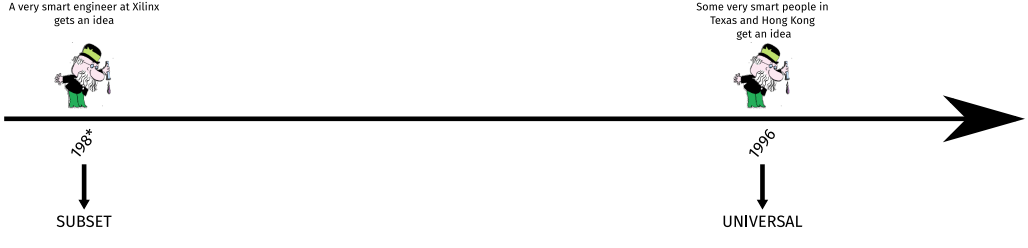

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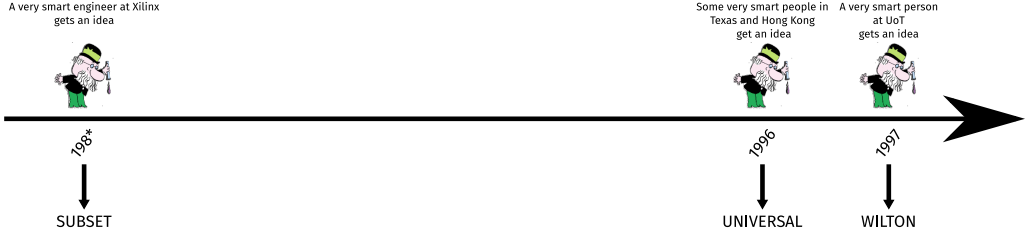
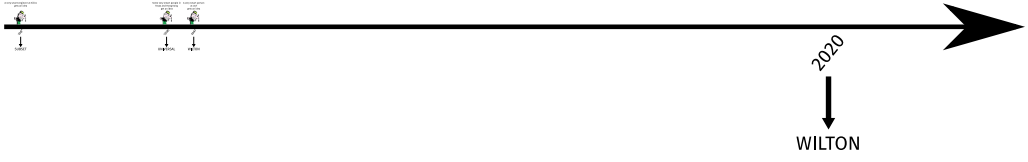


How Do We Explore FPGA Architecture?

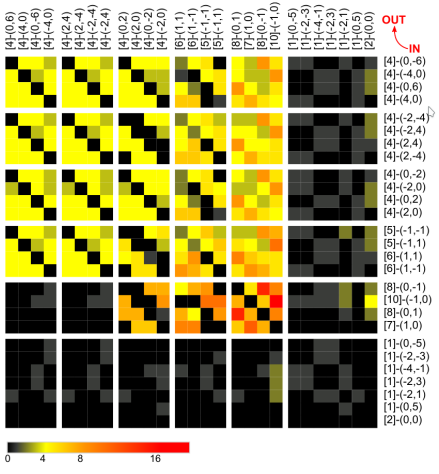
What about Switch-Block Patterns? (apologies for a bit of an exaggeration)



Meanwhile in Industry…

NetCracker: A Peek into the Routing Architecture of Xilinx 7-Series FPGAs

Morten B. Petersen, Stefan Nikolić and Mirjana Stojilović



Different

Architectural Enhancements in Intel® Agilex™ FPGAs

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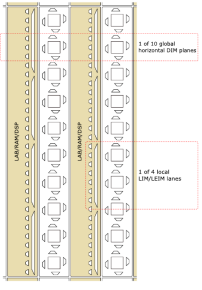

Difference increasing (Technology scaling)

How Do We Explore FPGA Architecture?

Can’t we automate SB-pattern exploration too?

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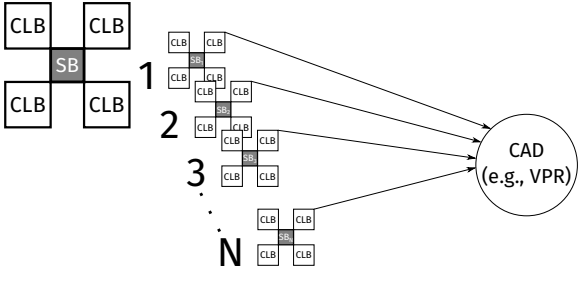

Sure!

How Do We Explore FPGA Architecture?

How big is N?

How Do We Explore FPGA Architecture?

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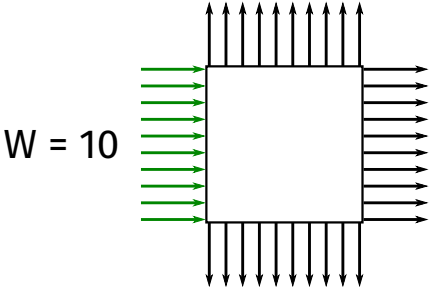
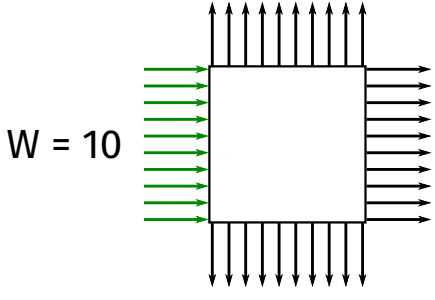


How Do We Explore FPGA Architecture?

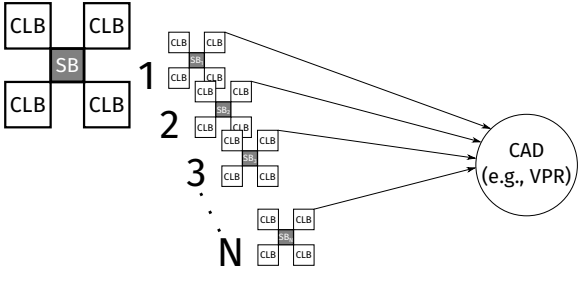
How big is N?



$$\sum_{k=10}^{30} \binom{30}{k} \cdot 10! \cdot \left\{ {k \atop 10} \right\} \qquad \sim 10^{31}$$

How Do We Explore FPGA Architecture?

Can’t we automate SB-pattern exploration too?



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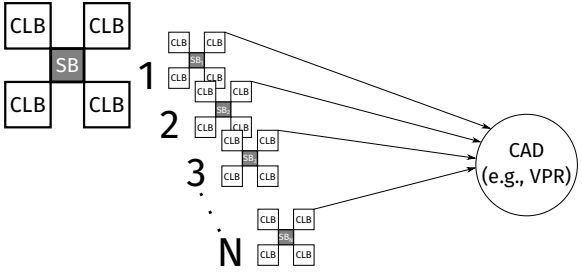
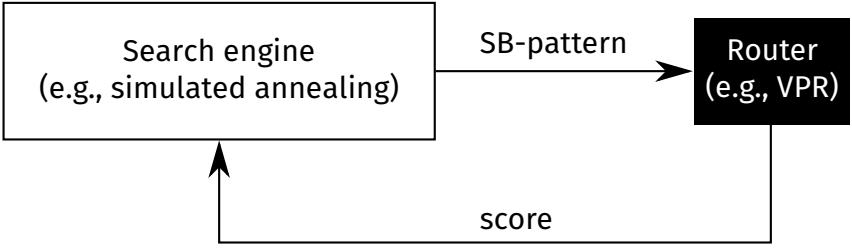


Surely not like this!

Automated Switch-Pattern Exploration

An Intuitive Solution: Iterative Improvement



[1] M. Lin, J. Wawrzynek, and A. El Gamal, “Exploring FPGA routing architecture stochastically”, TCAD’10

Using the router as a black box

to evaluate enumerated solutions

is inefficient

This inefficient...

A Little Analogy

You enter a restaurant and order a soup.

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Waiter: “How do you find the taste of the soup sir, on scale 0–9?”

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The waiter goes away with your soup, adds some salt and comes back.

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You enter a restaurant and order a soup.

Waiter: “How do you find the taste of the soup sir, on scale 0–9?”
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The waiter goes away with your soup, adds some salt and comes back.

Waiter: “Please try it now sir.”
You: “4”

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You: “4”

The waiter disappears with the soup again and adds some pepper.

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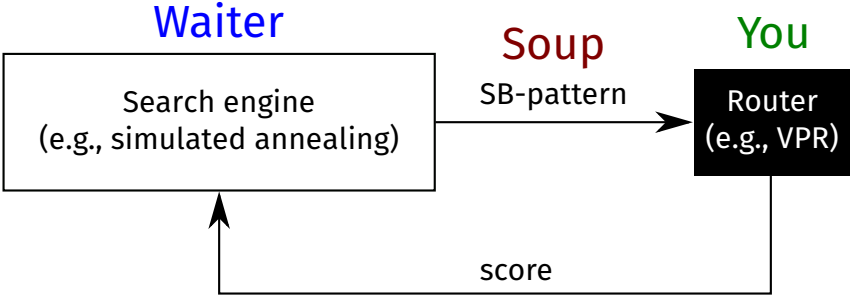
The waiter disappears with the soup again and adds some pepper.

Waiter: “How about now sir?”
You: “3”

The waiter disappears yet again, but this time you leave the table too.

A Little Analogy



A Little Analogy

Now something that we are a bit more accustomed to:

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A Little Analogy

Now something that we are a bit more accustomed to:

You enter a restaurant and order a soup.

Waiter: “Here you go sir, and here are all the spices we have available, in case you miss something.”

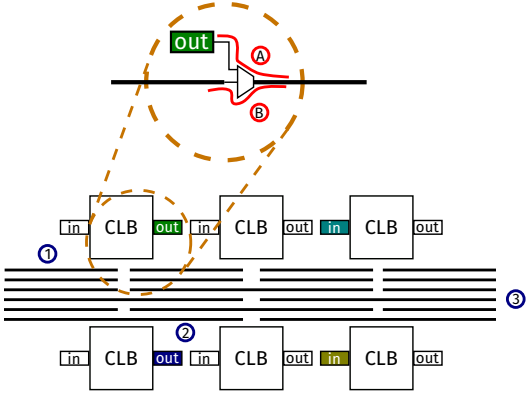
You try the soup and add a bit of each spice that the waiter gave you, according to your taste and habit.

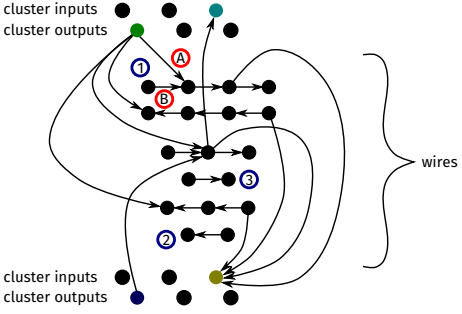
Can the router
spice up its own soup?

Can the router
design the switch-pattern?

A Quick Recap on FPGA Routers

Representing an FPGA as a Graph





Each node has a cost

Very Simplified Algorithm

```
repeat
    foreach CONNECTION IN THE CIRCUIT do
        route using shortest path in the RR-graph;

        update node costs;


    end
until OVERUSED NODES EXIST;
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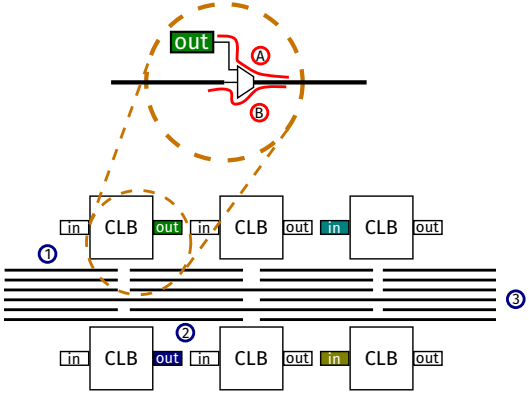

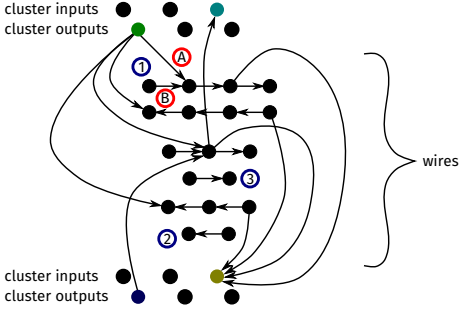

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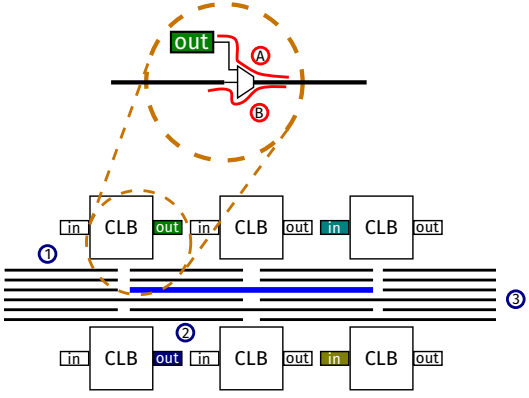

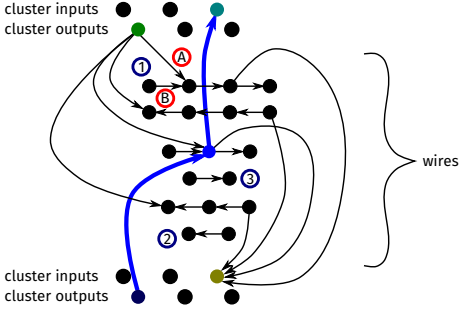

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repeat
    foreach CONNECTION IN THE CIRCUIT do
        route using shortest path in the RR-graph;
        (different signals can overlap)
        update node costs;

    end
until OVERUSED NODES EXIST;
```
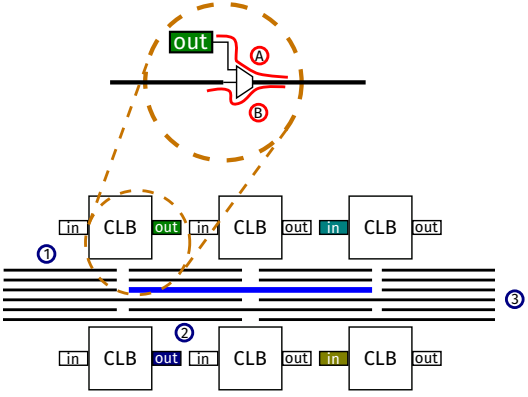
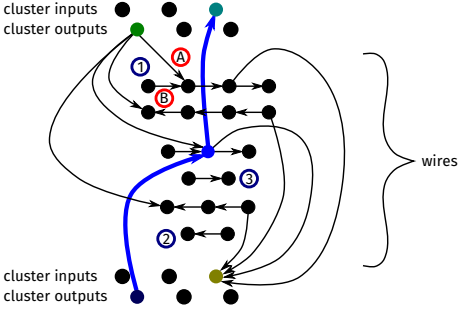

Very Simplified Algorithm





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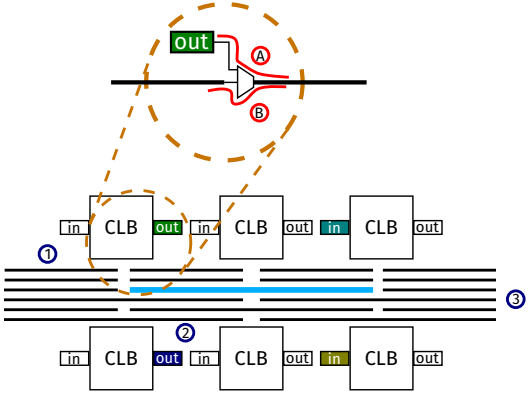

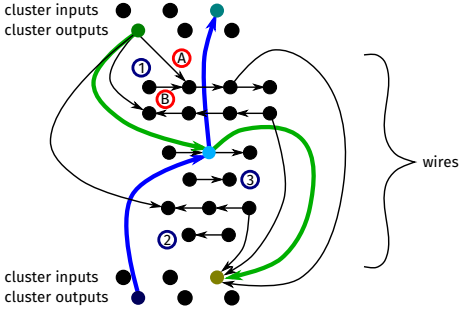

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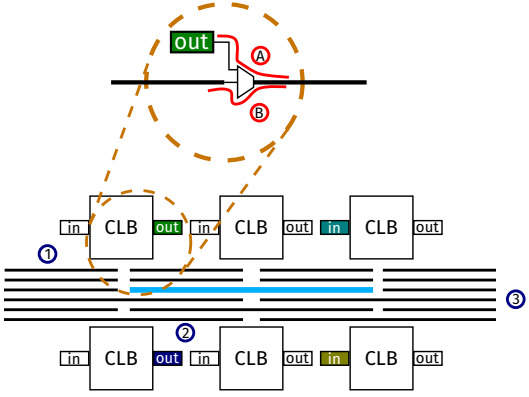

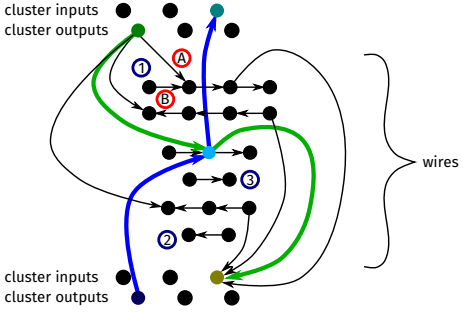

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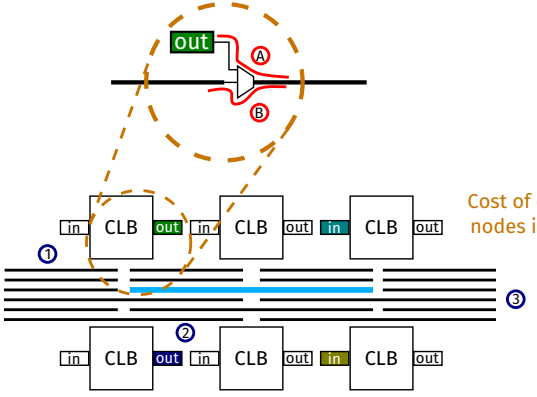
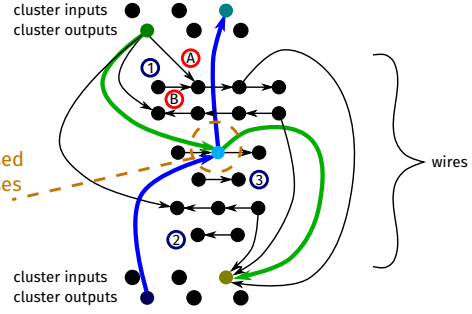


Cost of overused nodes increases



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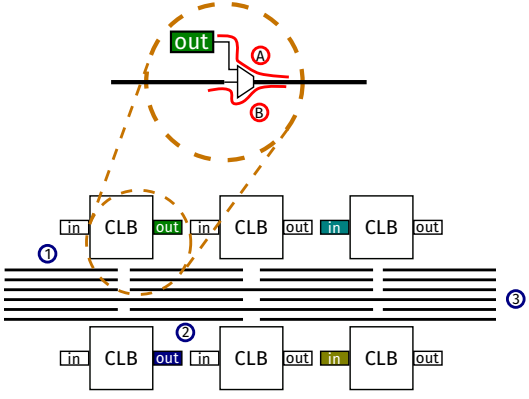
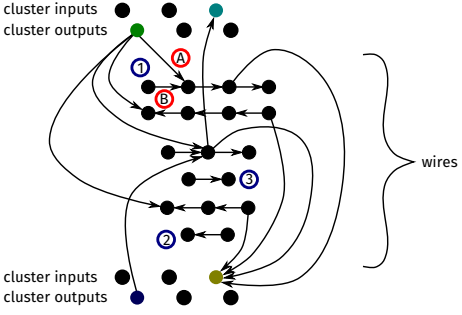
```
repeat
    foreach CONNECTION IN THE CIRCUIT do
        route using shortest path in the RR-graph;
        (different signals can overlap)
        update node costs;
    end
    update node costs;
    throw away all routing (rip-up);
until OVERUSED NODES EXIST;
```

Very Simplified Algorithm





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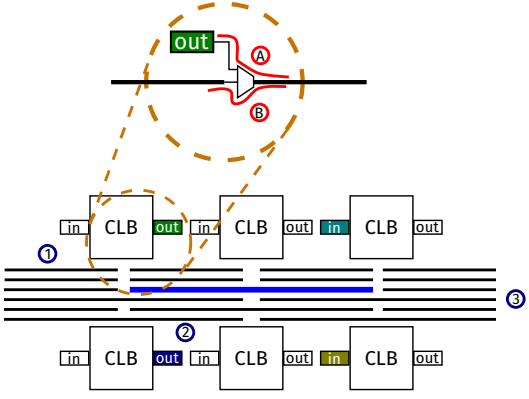

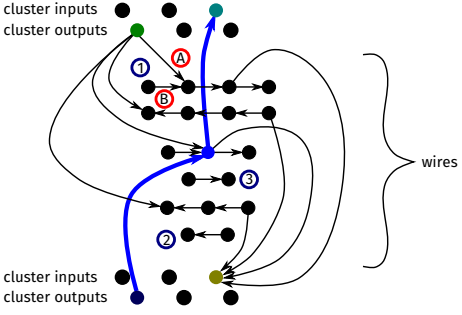

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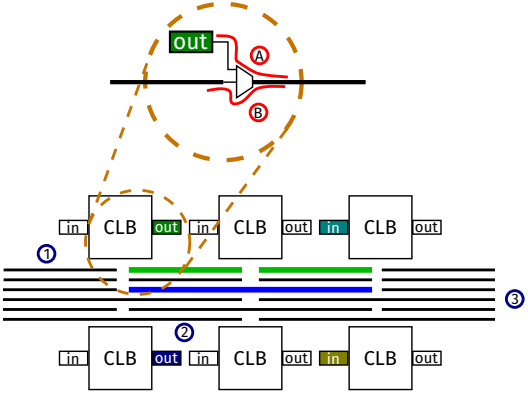
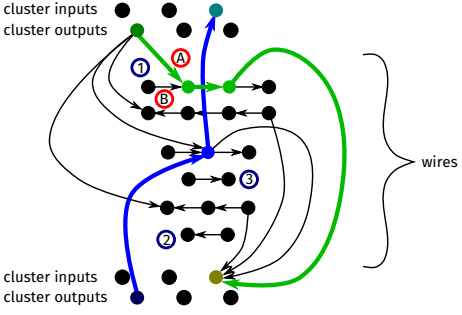
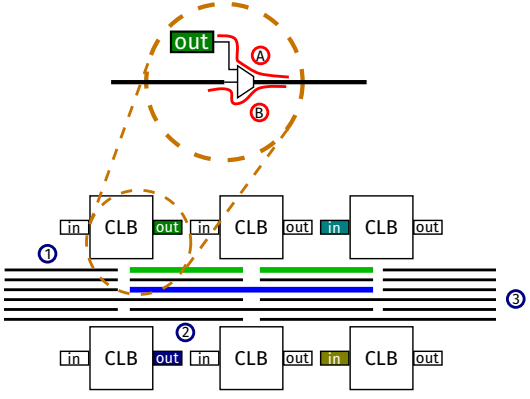


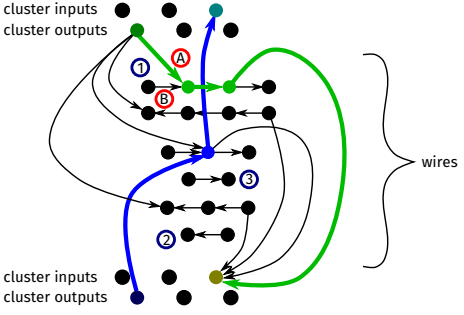


Each node has a cost

Very Simplified Algorithm

Signals negotiate which one will give up its desired nodes

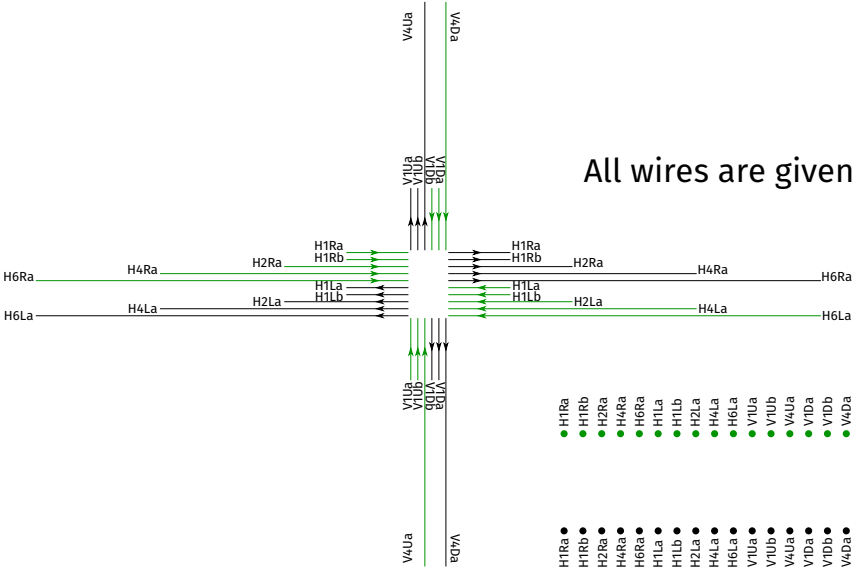




Each node has a cost

Negotiating Switch Presence

Letting the Router Design the SB-Pattern



All wires are given

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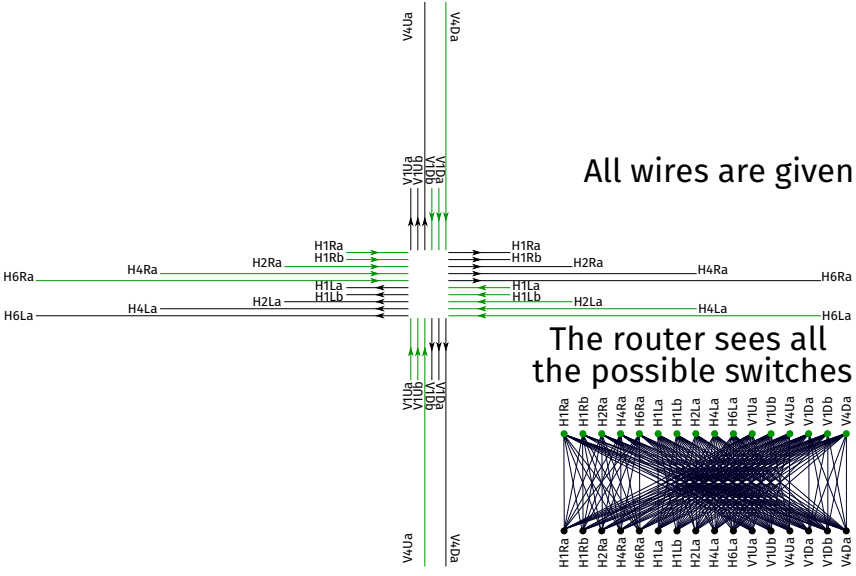
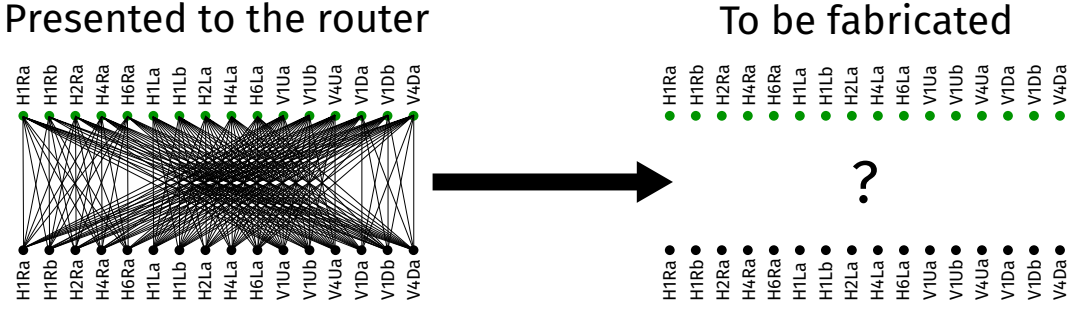


All wires are given

The router sees all the possible switches

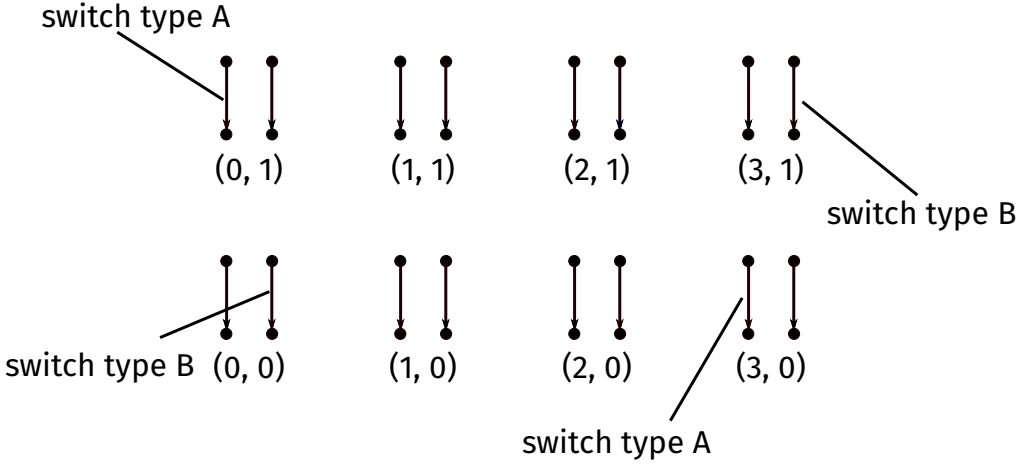
Letting the Router Design the SB-Pattern



Use the router's decisions to select switches for fabrication

A Simple Greedy Solution

Usage(*e*) = # SB instances (tiles) in which a switch *type e* is used.



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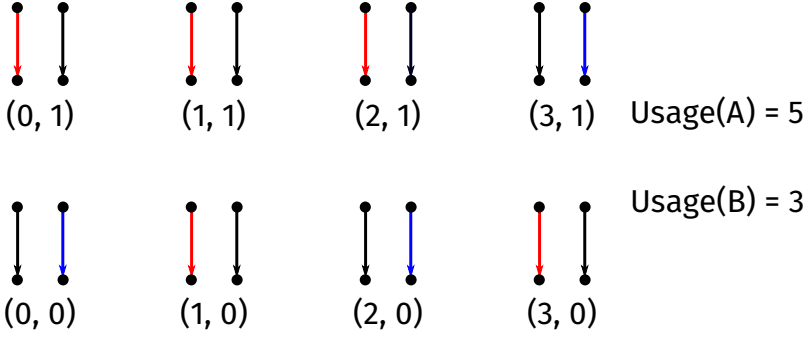

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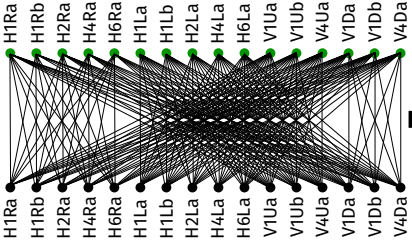
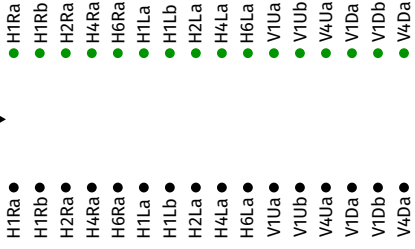
Letting the Router Design the SB-Pattern

Presented to the router



To be fabricated



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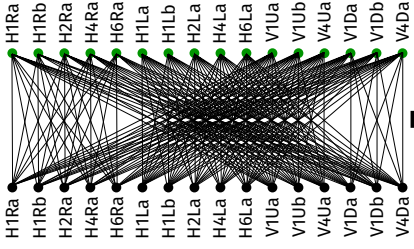

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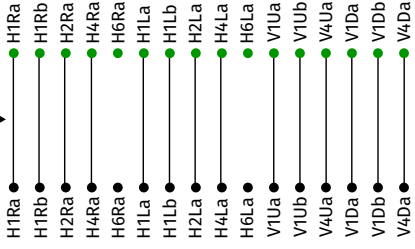

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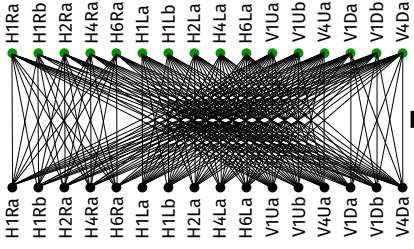

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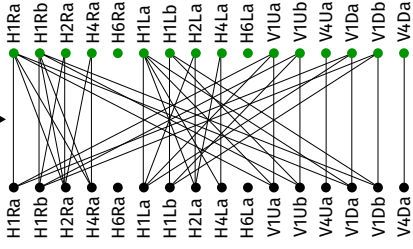

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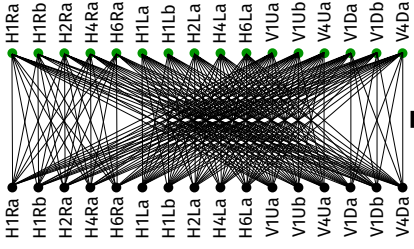

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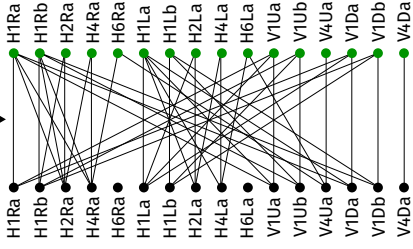

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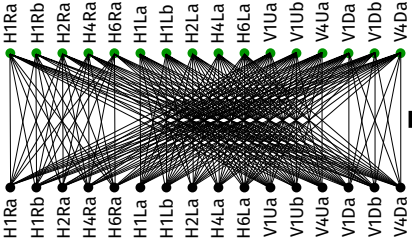

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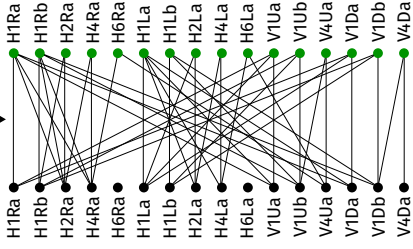
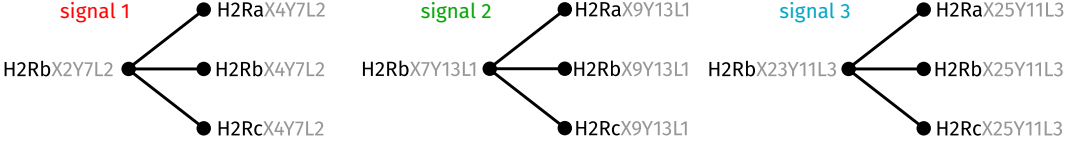


A Simple Greedy Solution: Failure



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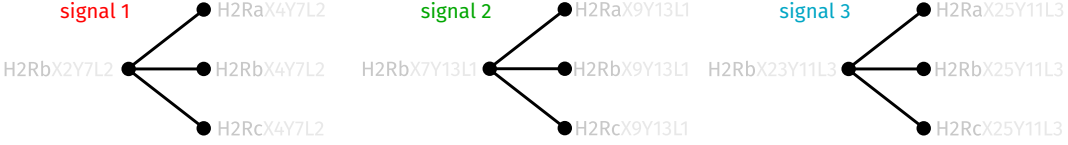

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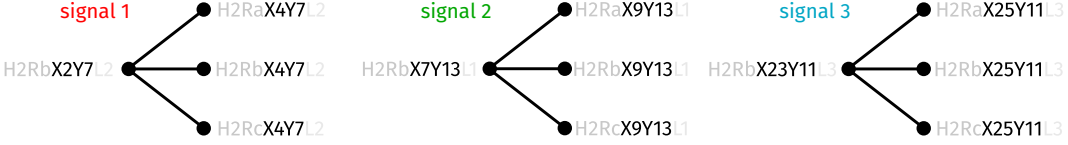

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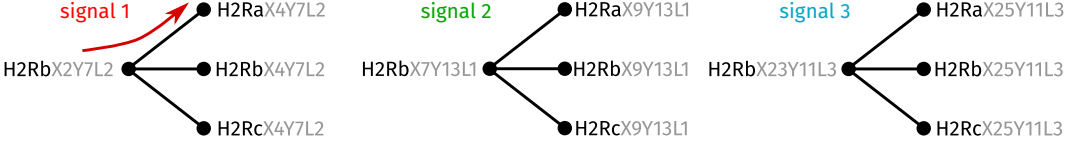

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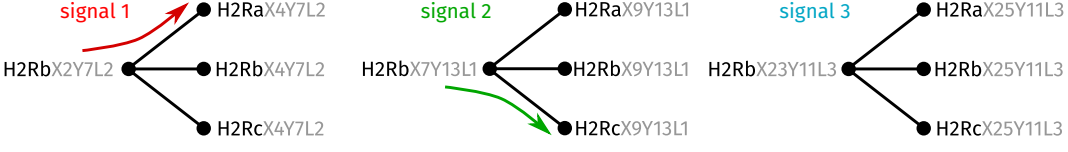

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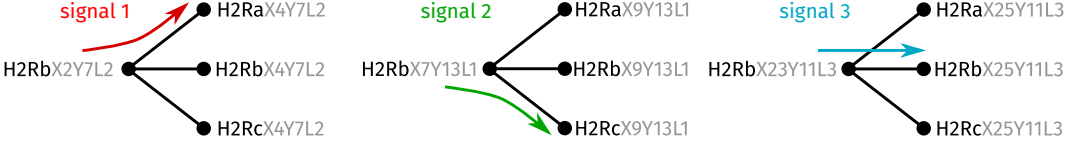

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Must take all three switch types from the example

Avalanche Costs (Key Idea)

Avalanche Costs: Rationale

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Avalanche Costs: Rationale

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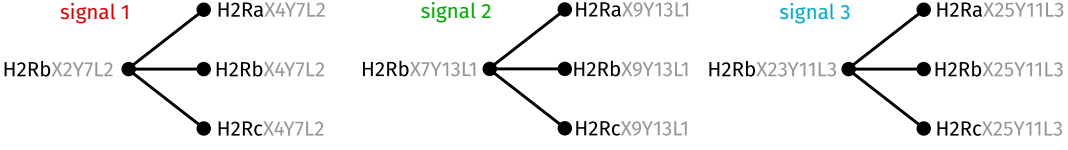

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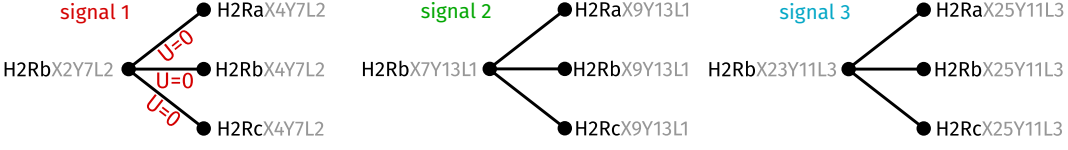

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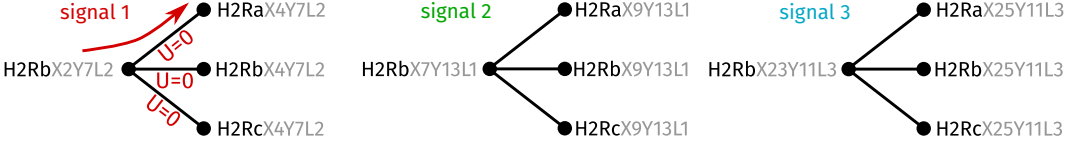

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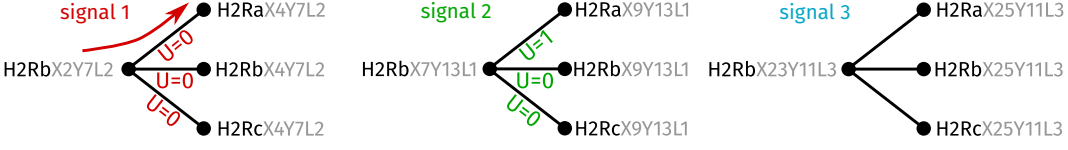

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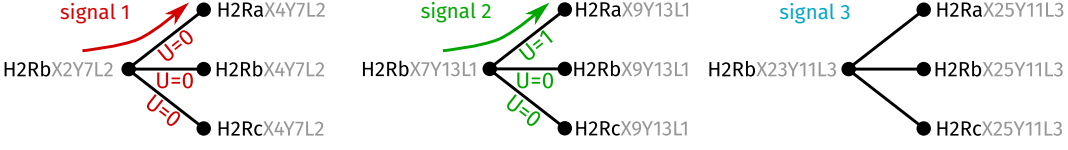

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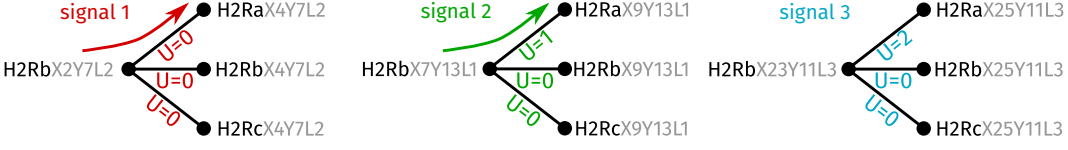

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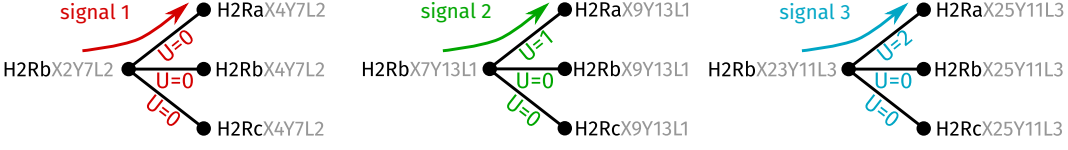

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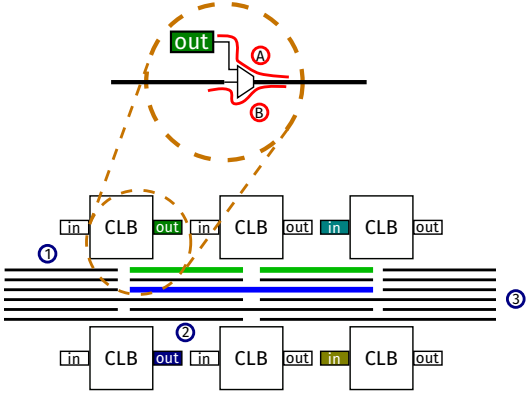
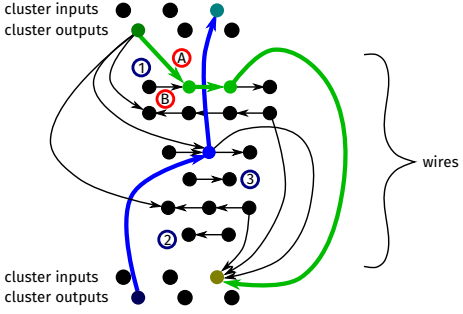
After rip-up, more signals move to switches with higher Usage, creating an avalanche effect

Avalanche Costs: Similarity with Congestion Negotiation

Signals negotiate which one will give up its desired nodes





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Circuit Routing with Pathfinder

SB-Pattern Design with Avalanche Costs

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Spreads the routes over more wire **instances**	
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$\Longrightarrow$ congestion-free routing

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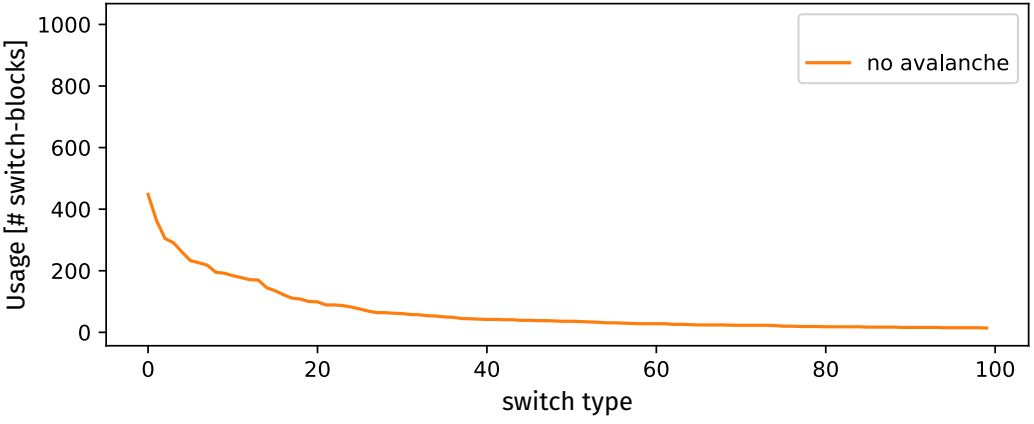
Circuit Routing with Pathfinder	SB-Pattern Design with Avalanche Costs
Spreads the routes over more wire **instances**	Concentrates the routes on fewer switch **types**
$\Longrightarrow$ congestion-free routing	$\Longrightarrow$ optimizes the switch-pattern

Avalanche Costs: Effects



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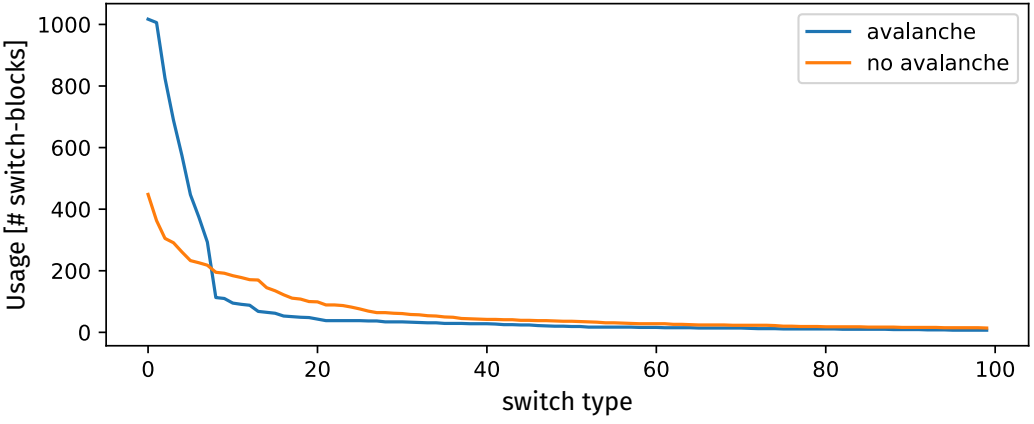

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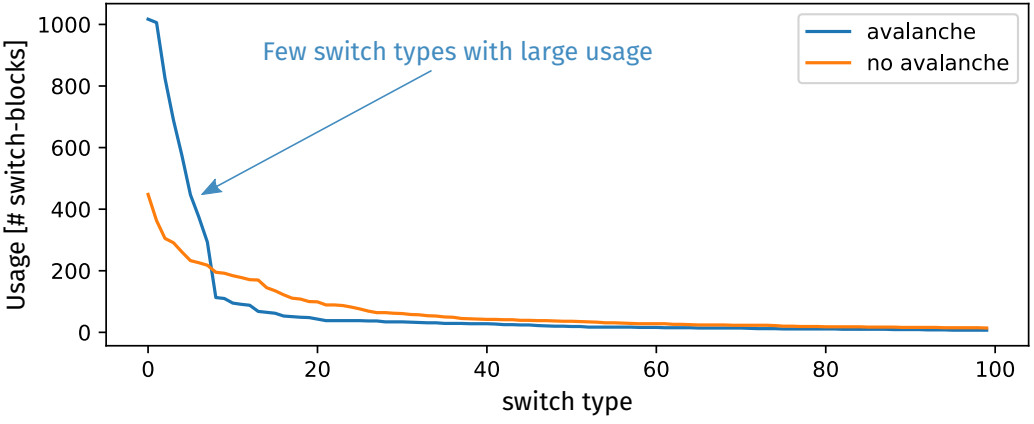

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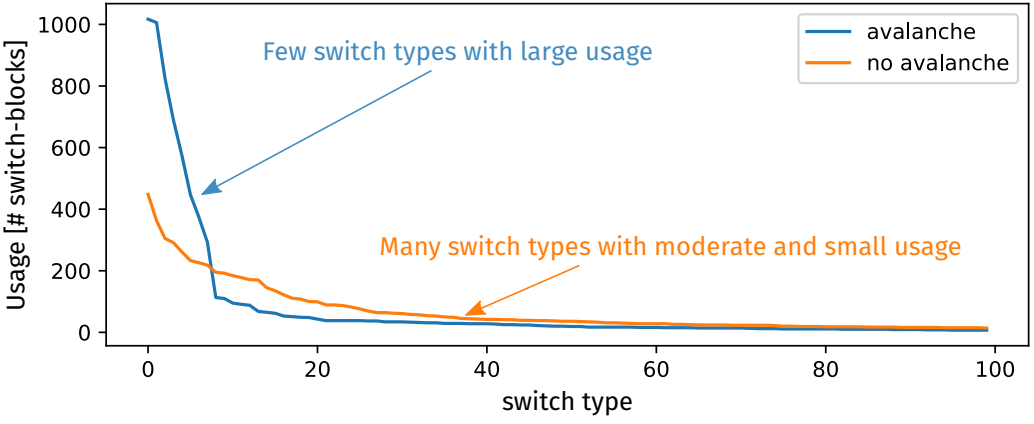

The Complete Algorithm

Very similar to Simple Greedy:

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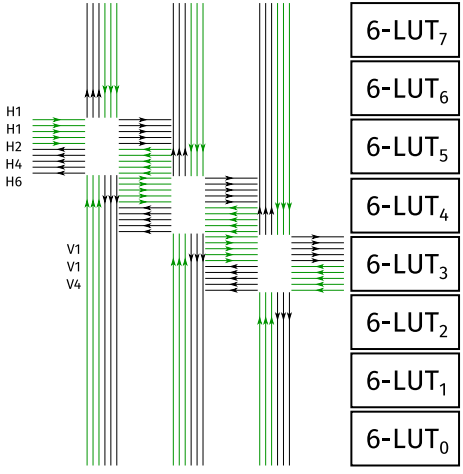
More details in the paper

Experimental Results

Experimental Setup



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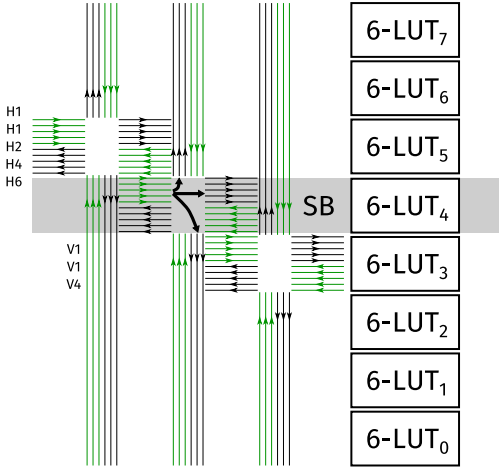

SB defined at LUT level

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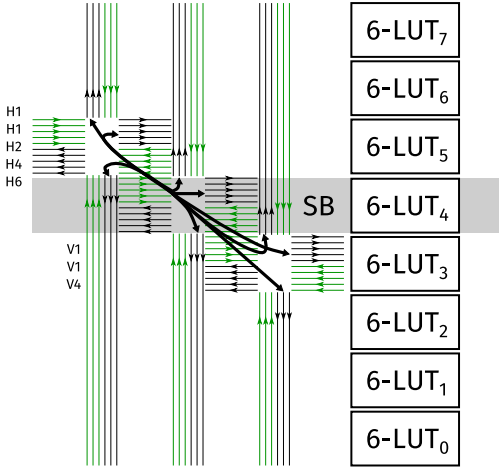

SB defined at LUT level

Switches allowed between adjacent LUTs

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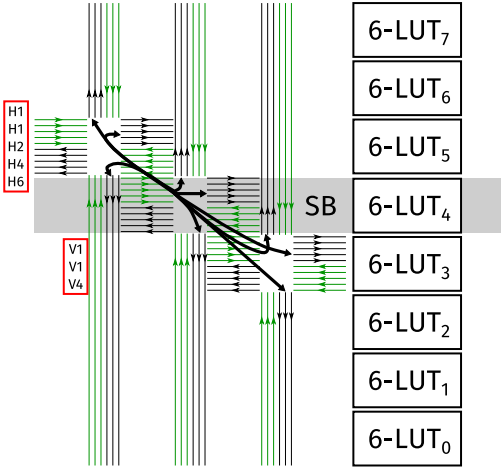

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564 potential switch types

Comparison with Greedy

	avalanche			greedy		
#iterations	63			228		
#switches	93			438		
	fi_{avg}	fo_{avg}	t_{avg} [ps]	fi_{avg}	fo_{avg}	t_{avg} [ps]
H1	5	5	14.5	31	25	23.1
H2	5	5	17.8	28	28	31.6
H4	8	7	25.9	21	27	43.2
H6	6	6	34.9	19	25	59.6
V1	7	7	22.2	38	31	35.5
V4	5	8	71.7	12	27	97.5
W(tile)	6816 nm			8904 nm		
CPD	1.40 ns			1.71 ns		

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H1	5	5	14.5	31	25	23.1
H2	5	5	17.8	28	28	31.6
H4	8	7	25.9	21	27	43.2
H6	6	6	34.9	19	25	59.6
V1	7	7	22.2	38	31	35.5
V4	5	8	71.7	12	27	97.5
W(tile)	6816 nm			8904 nm		
CPD	1.40 ns			1.71 ns		

Comparison with Greedy

	avalanche			greedy		
#iterations	63			228		
#switches	93			438		
	fi_{avg}	fo_{avg}	t_{avg} [ps]	fi_{avg}	fo_{avg}	t_{avg} [ps]
H1	5	5	14.5	31	25	23.1
H2	5	5	17.8	28	28	31.6
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Comparison with Greedy

	avalanche			greedy			truncated greedy		
#iterations	63			228			62		
#switches	93			438			92		
	fi_{avg}	fo_{avg}	t_{avg} [ps]	fi_{avg}	fo_{avg}	t_{avg} [ps]	fi_{avg}	fo_{avg}	t_{avg} [ps]
H1	5	5	14.5	31	25	23.1	6	4	14.3
H2	5	5	17.8	28	28	31.6	7	6	18.4
H4	8	7	25.9	21	27	43.2	4	7	26.4
H6	6	6	34.9	19	25	59.6	2	7	35.9
V1	7	7	22.2	38	31	35.5	10	7	22.0
V4	5	8	71.7	12	27	97.5	2	5	67.8
W(tile)	6816 nm			8904 nm			7368 nm		
CPD	1.40 ns			1.71 ns			1.41 ns		

Comparison with Greedy

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#iterations	63			228			62		
#switches	93			438			92		
	fi_{avg}	fo_{avg}	t_{avg} [ps]	fi_{avg}	fo_{avg}	t_{avg} [ps]	fi_{avg}	fo_{avg}	t_{avg} [ps]
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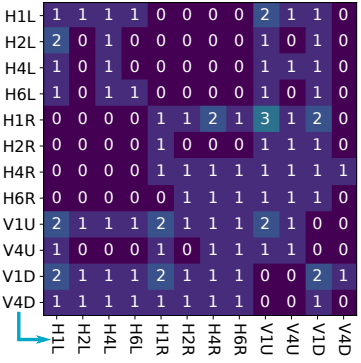
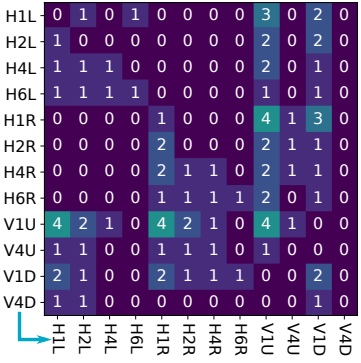
Avalanche vs Greedy: Switch Selection Choices

avalanche

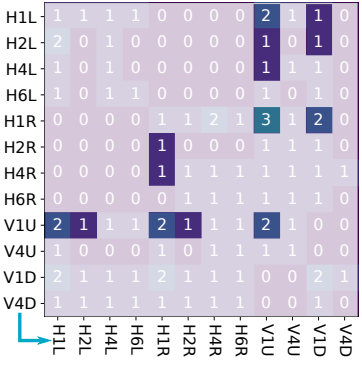


truncated greedy

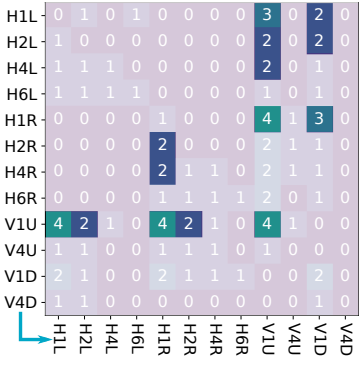


Avalanche vs Greedy: Switch Selection Choices

avalanche

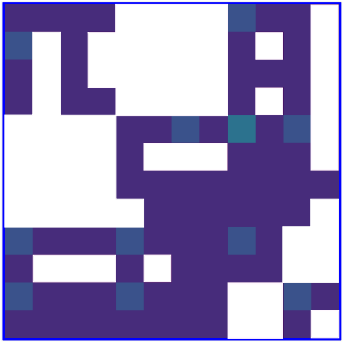


truncated greedy

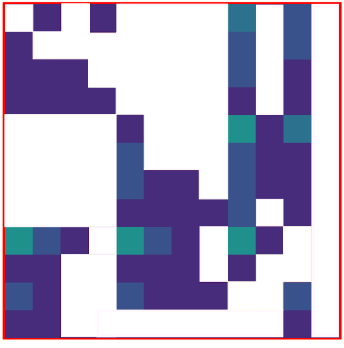


Avalanche vs Greedy: Switch Selection Choices

avalanche



truncated greedy



Avalanche vs Greedy: Routability

10 Gnl circuits

Rent's exponent = 0.7

10k LUT

avalanche	147	145	57	73	56	71	82	59	65	74
trunc. greedy	—	—	—	—	278	—	—	—	149	—

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10 Gnl circuits

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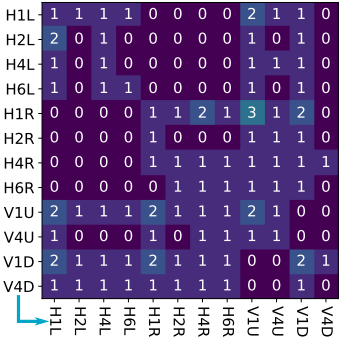
avalanche	147	145	57	73	56	71	82	59	65	74
trunc. greedy	—	—	—	—	278	—	—	—	149	—

Comparison with Simulated Annealing

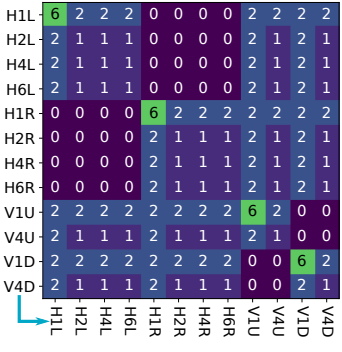
Inspired by M. Lin, J. Wawrzynek, and A. El Gamal,
“Exploring FPGA routing architecture stochastically”, TCAD’10

Comparison with Simulated Annealing: Starting Pattern

avalanche



ISFPGA'21



[1] S. Nikolić, F. Catthoor, Z. Tőkei, and P. Ienne,
“Global is the New Local: FPGA Architecture at 5nm and Beyond”, FPGA’21

Comparison with Simulated Annealing: Setup

- Each move is an exclusion/inclusion of one of the 564 switch types

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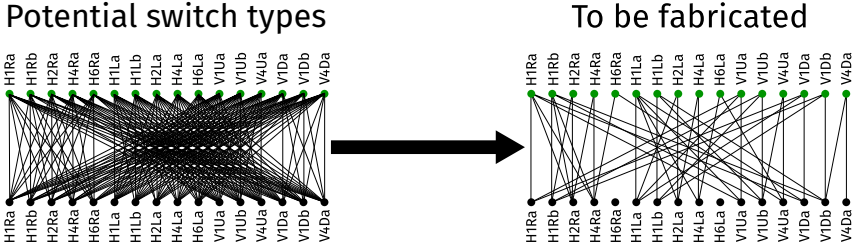

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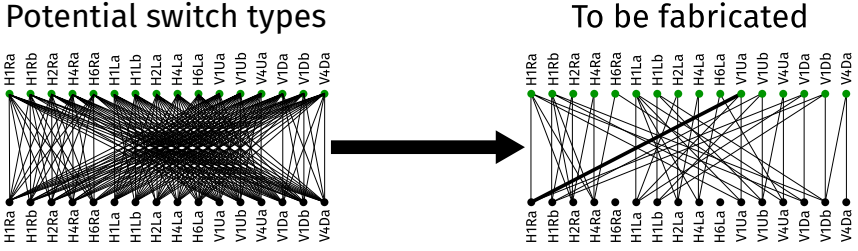

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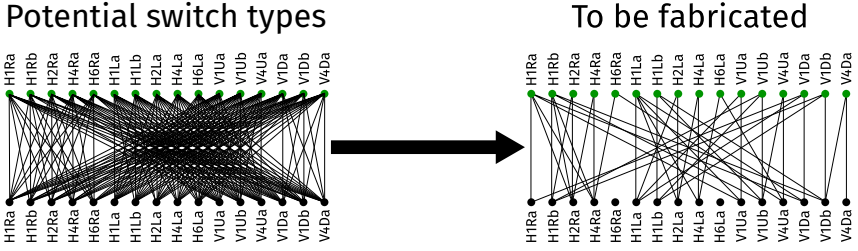

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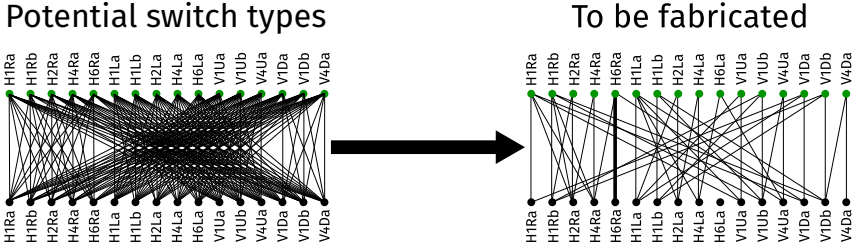

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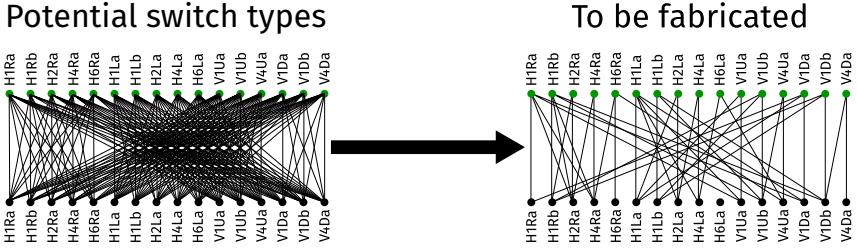

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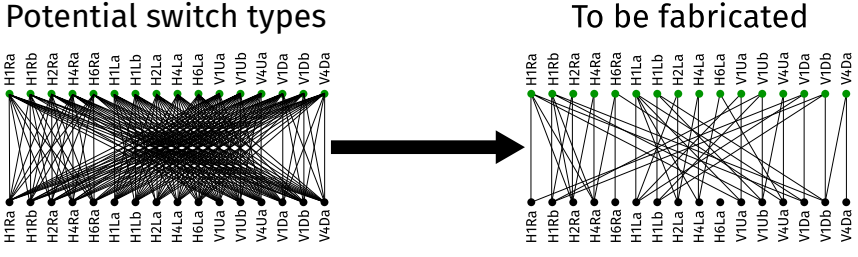
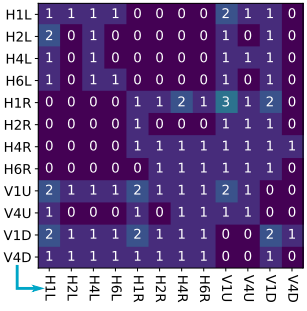


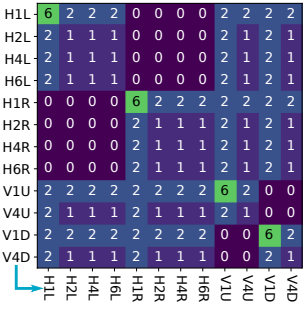
- cost function = f(CPD, tile area)

Comparison with Simulated Annealing: Outcome

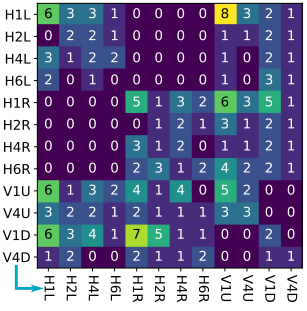
avalanche



ISFPGA'21



annealed



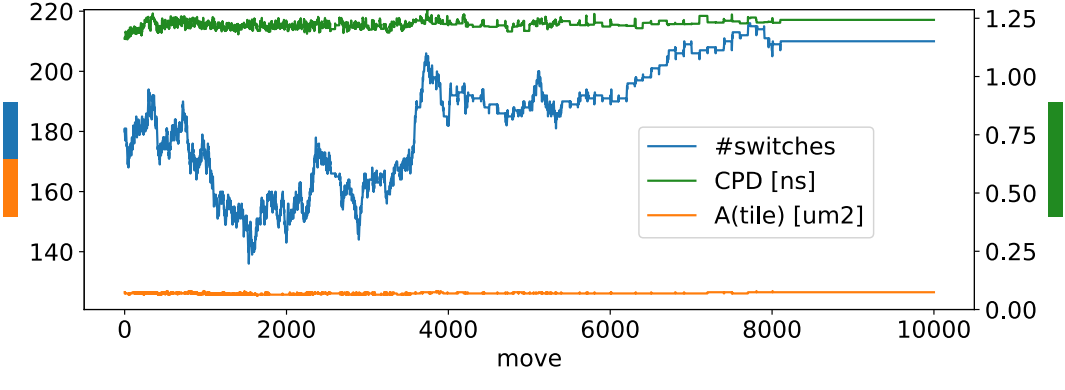
+ 30 switches

Comparison with Simulated Annealing: Outcome

	avalanche			initial			annealed		
#switches	93			180			210		
	fi_{avg}	fo_{avg}	t_{avg} [ps]	fi_{avg}	fo_{avg}	t_{avg} [ps]	fi_{avg}	fo_{avg}	t_{avg} [ps]
H1	5	5	14.5	10	10	16.0	13	13	19.6
H2	5	5	17.8	11	11	21.3	14	11	24.1
H4	8	7	25.9	11	11	30.8	16	12	32.1
H6	6	6	34.9	11	11	43.1	9	13	47.3
V1	7	7	22.2	12	12	24.6	14	15	29.2
V4	5	8	71.7	13	13	74.3	13	15	86.8
W(tile)	6816 nm			7464 nm			7488 nm		
CPD	1.40 ns			1.46 ns			1.55 ns		

+ 10.7%

Simulated Annealing: Convergence



Conclusions and Future Work

FPGA routers can efficiently explore switch-block patterns

Future Work

Avalanche costs can be attributed to any node in any graph

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Avalanche costs can be attributed to any node in any graph

$\Longrightarrow$ use them to explore the entire routing architecture at once

Thank you for attention

https://github.com/EPFL-LAP/fpl21-avalanche