Global is the New Local:

FPGA Architecture at 5nm and Beyond

S. Nikolić, F. Catthoor*, Z. Tőkei*, and P. Ienne

FPGA'21, Online, 01.03.2021

École Polytechnique Fédérale de Lausanne
*IMEC

Metal Stack Evolution

N16: Wu et al.,

"A 16nm FinFET CMOS technology for mobile SoC and computing applications",

IEDM'13

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"A 7nm CMOS platform technology featuring 4th generation FinFET transistors with a 0.027 um2 high density 6-T SRAM cell for mobile SoC applications",

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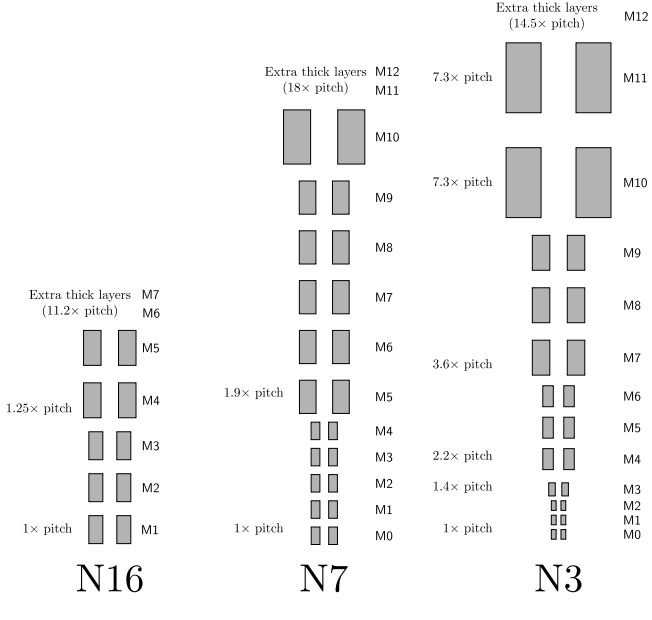

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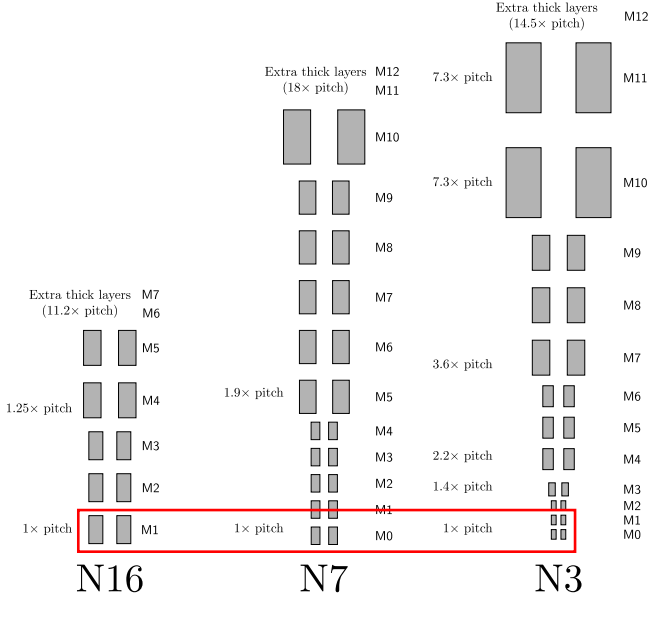
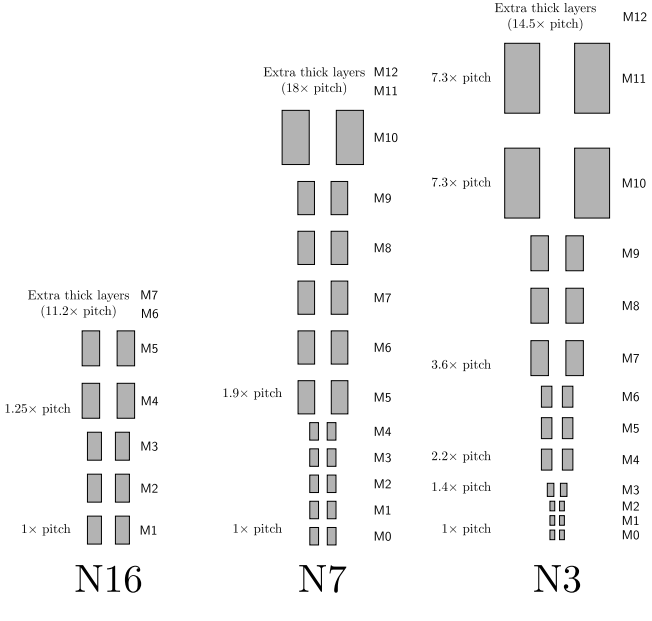


Some High School Physics

$$R = \frac{\rho l}{S}$$



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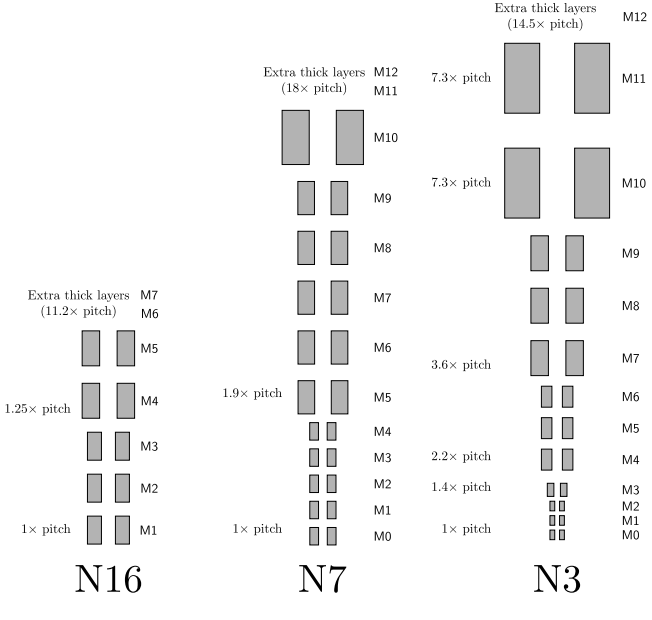

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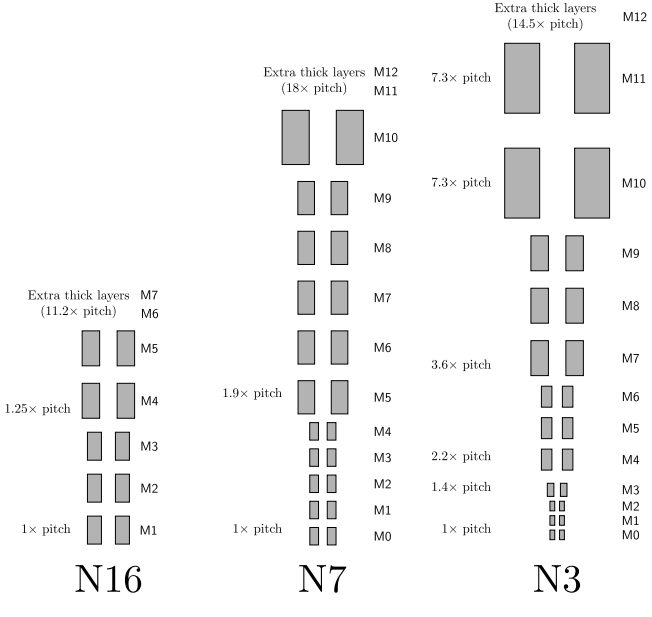

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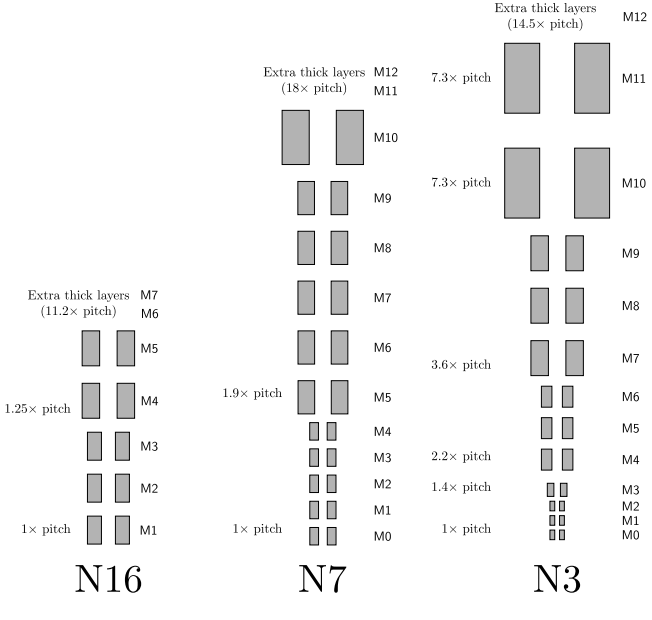
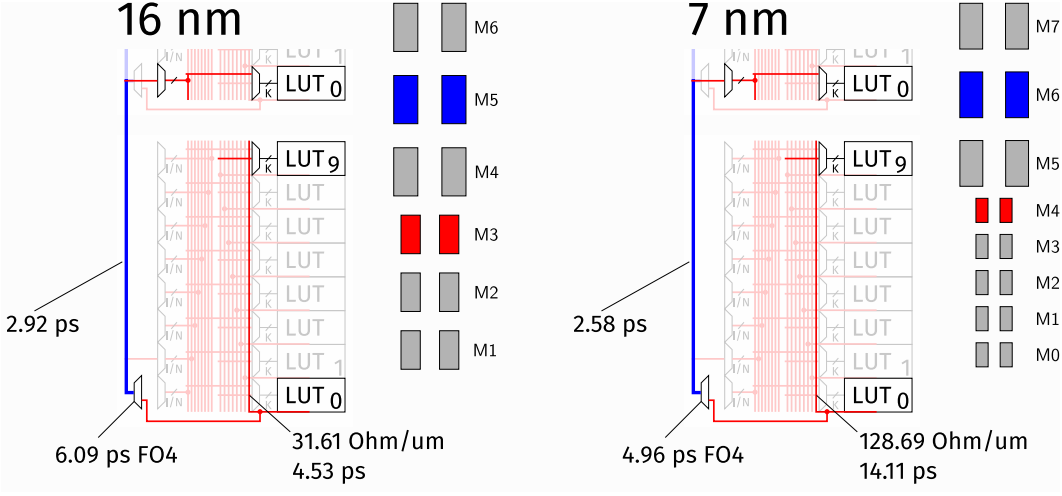


An Illustrative Example



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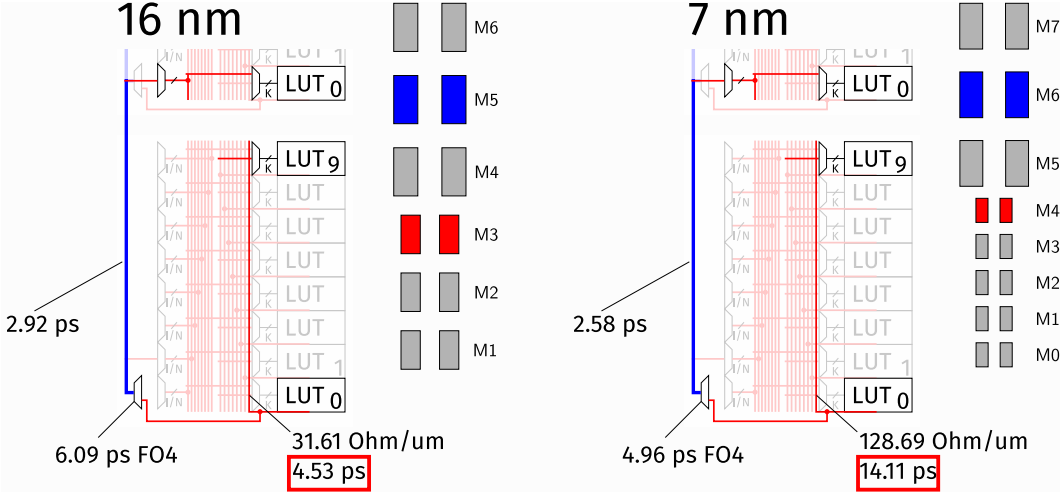

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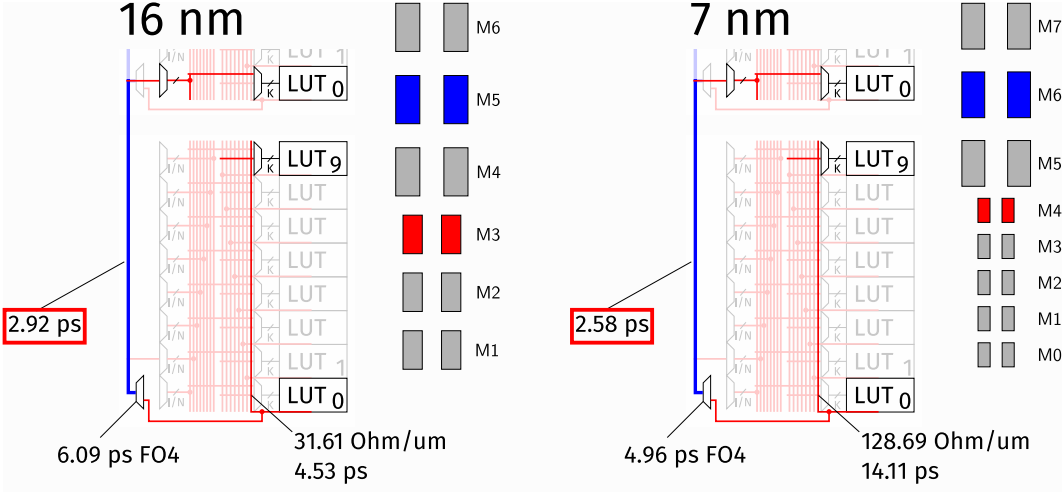

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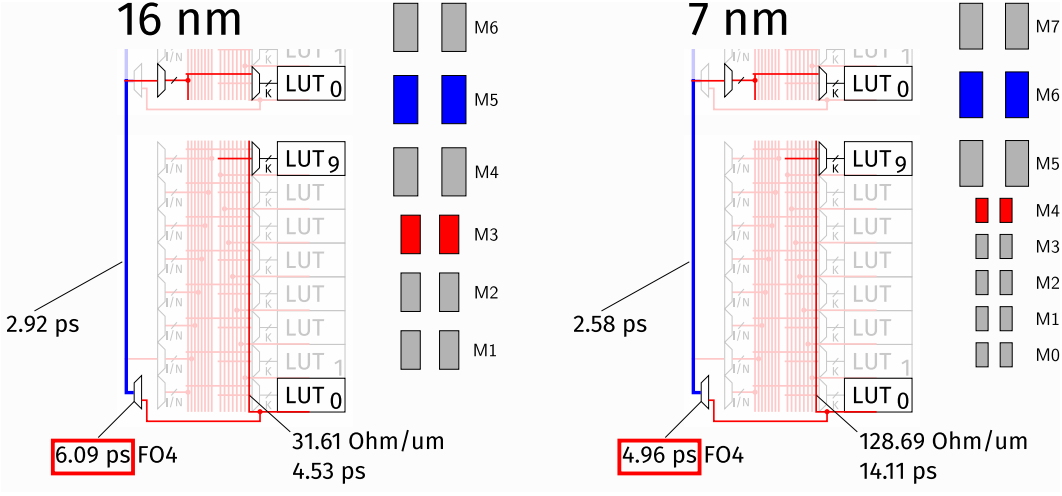

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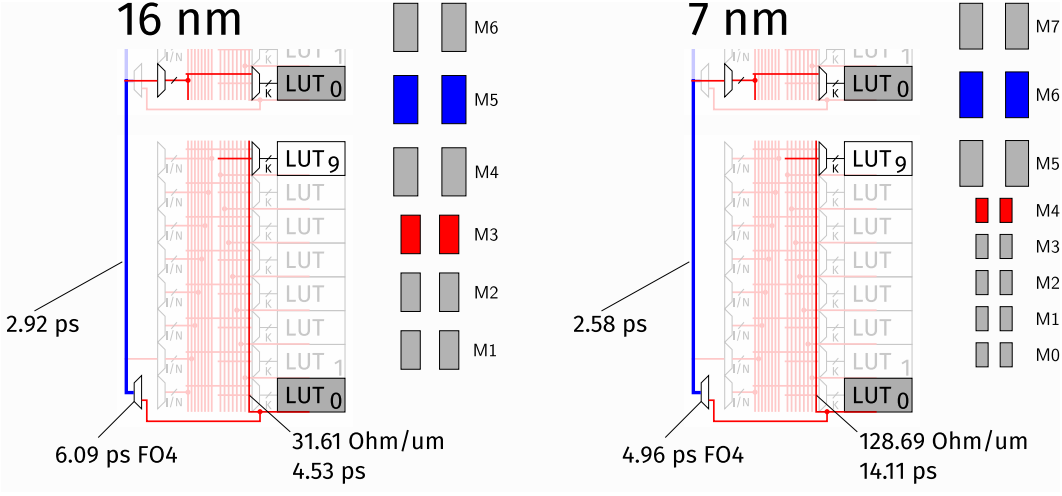

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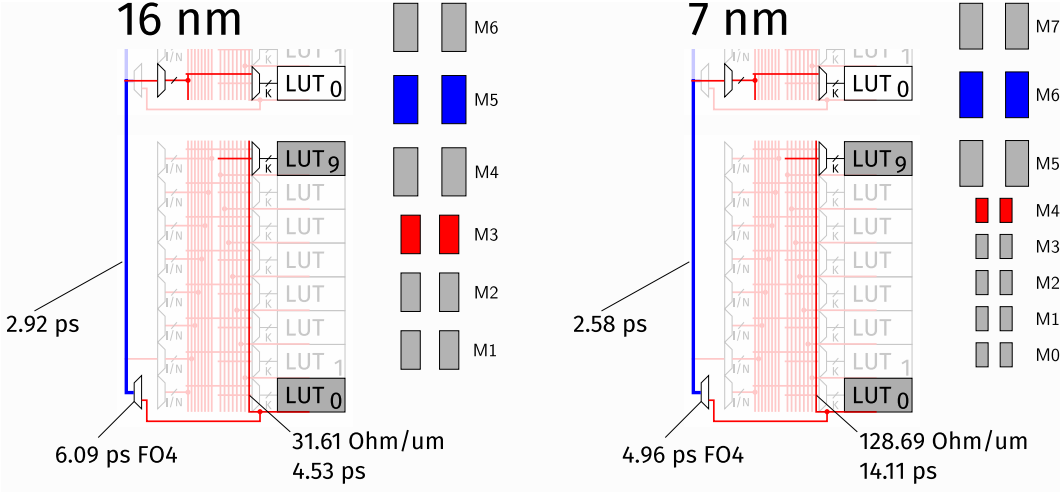


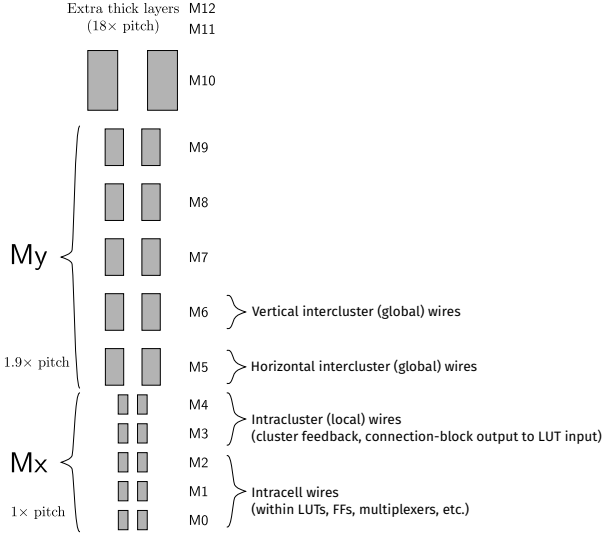
Outline

Metal Stack Modeling

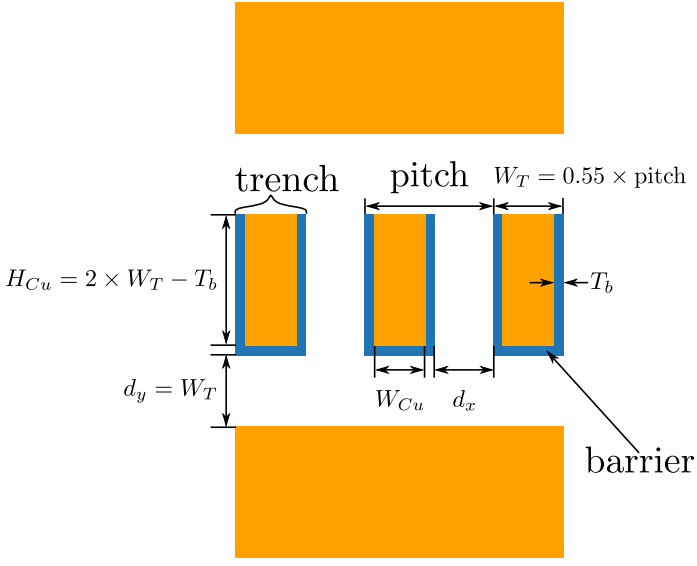
Layer Planning

Two pitch options considered:

- Mx for intracluster (local) wires
- My for intercluster (global) wires



Wire Geometry



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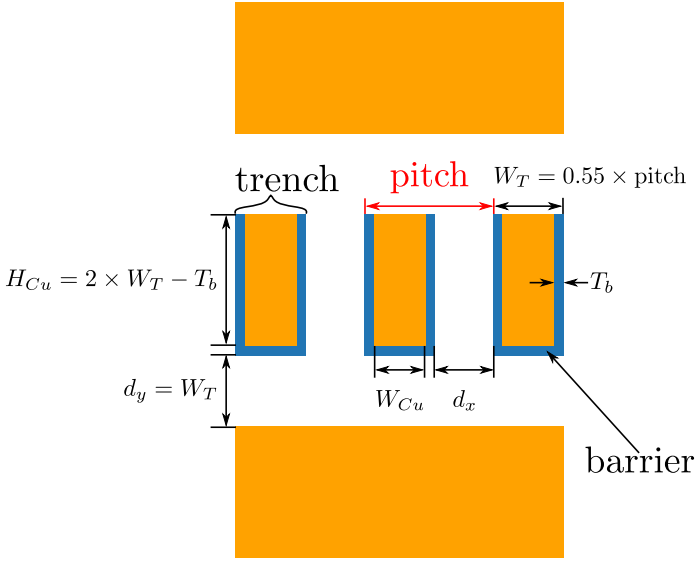
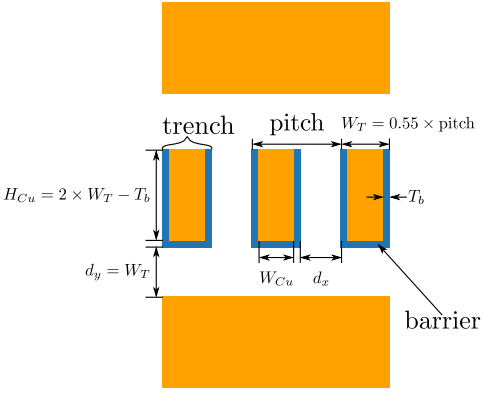


Resistance

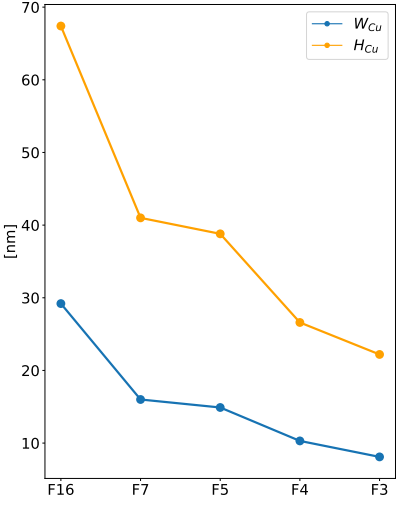


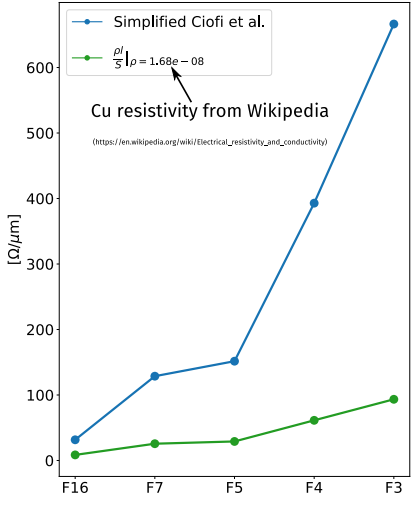
Ciofi et al., “Impact of Wire Geometry on Interconnect RC and Circuit Delay”, T-ED, 2016

$$R' = \frac{1}{H_{Cu} W_{Cu}} \left(32.05 + 615 \left(\frac{\tanh(0.133 W_{Cu})}{W_{Cu}} + \frac{\tanh(0.133 H_{Cu})}{H_{Cu}} \right) \right) \quad (1)$$

Resistance: Mx-Wires

	F16	F7	F5	F4	F3
pitch [nm]	64	40	38	26	22





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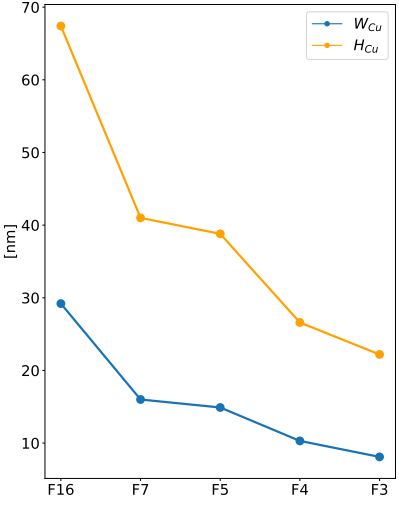

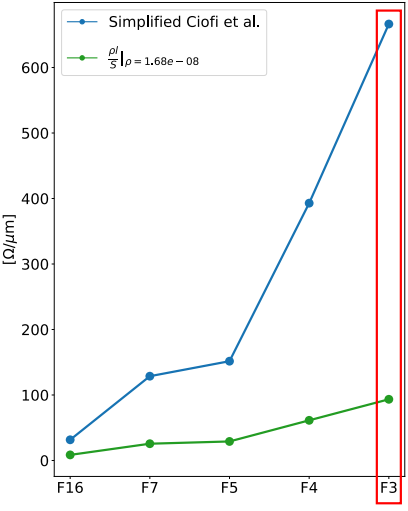

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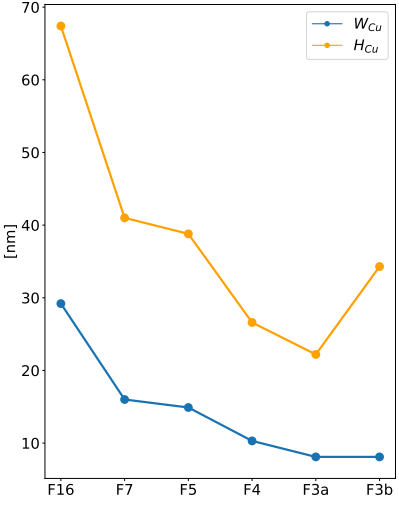

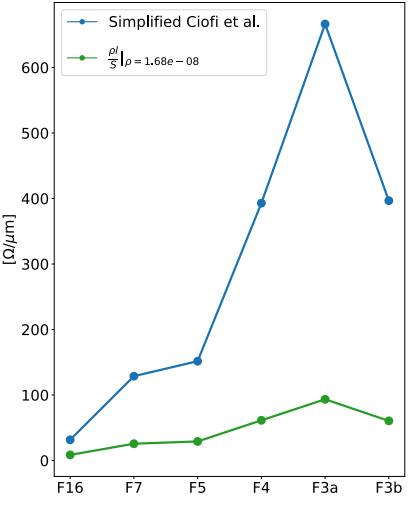

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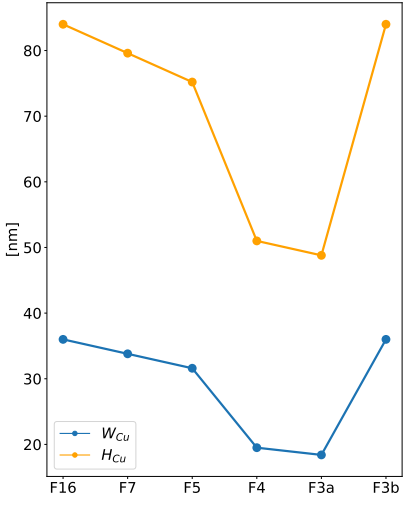

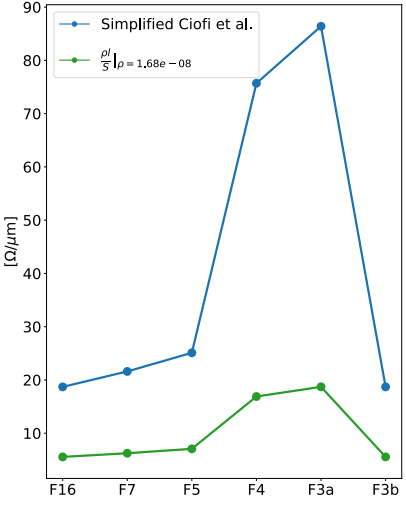

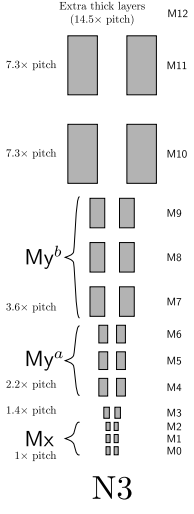

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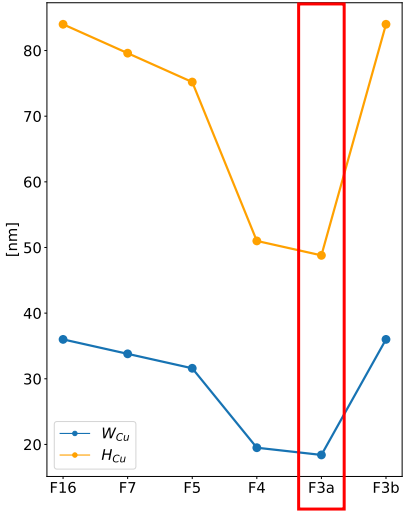

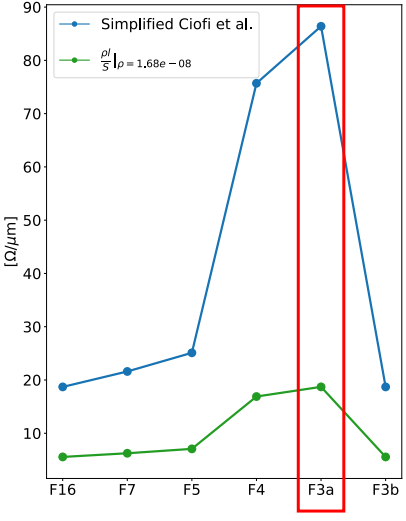

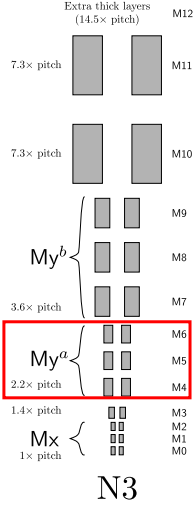

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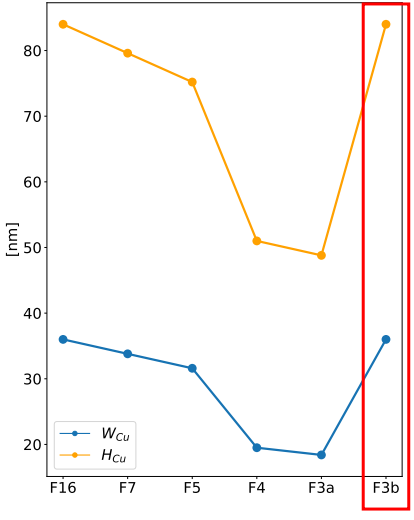

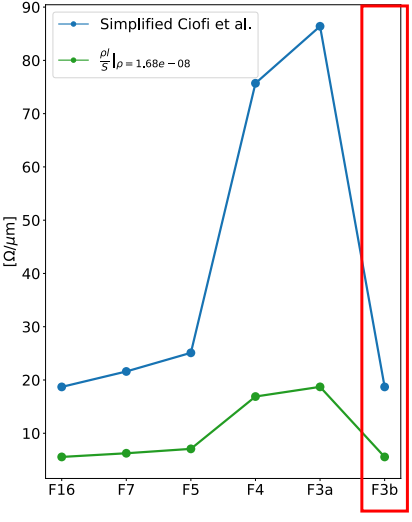

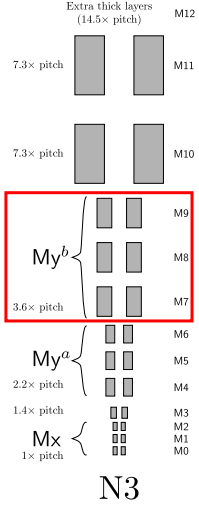

N3

Capacitance

- Capacitance is less sensitive to scaling than resistance

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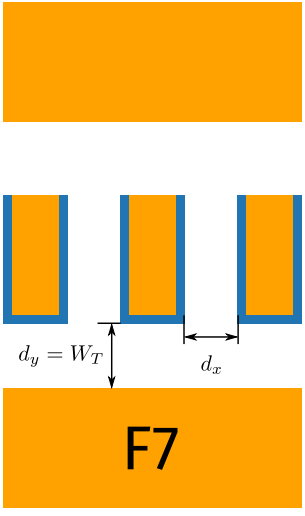

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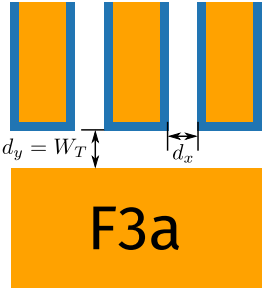
$$d \nearrow \implies C \nearrow$$



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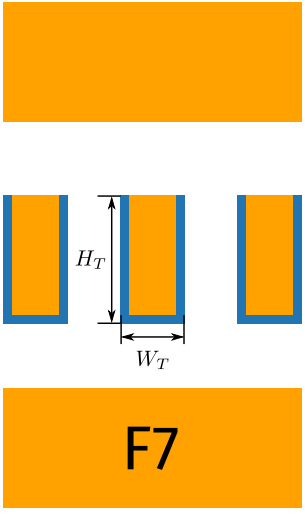

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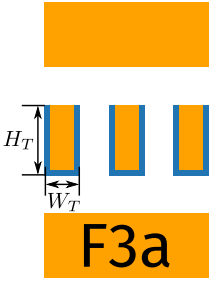


Capacitance

Wong et al., “Modeling of interconnect capacitance, delay, and crosstalk in VLSI”, T-SM, 2000

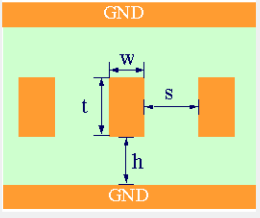
Predictive Technology Model

- Introduction
- Latest Models
- Nano-CMOS
- Post-Silicon
- Interconnect

INTERCONNECT

Structure 2

Coupling lines between two metal ground planes (for local and intermediate layers)



Predictive Technology Model (PTM), Nanoscale Integration and Modeling Group, Arizona State University (ptm.asu.edu)

Area and Wirelength Modeling

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Good area and length models are necessary for

- Delay measurement

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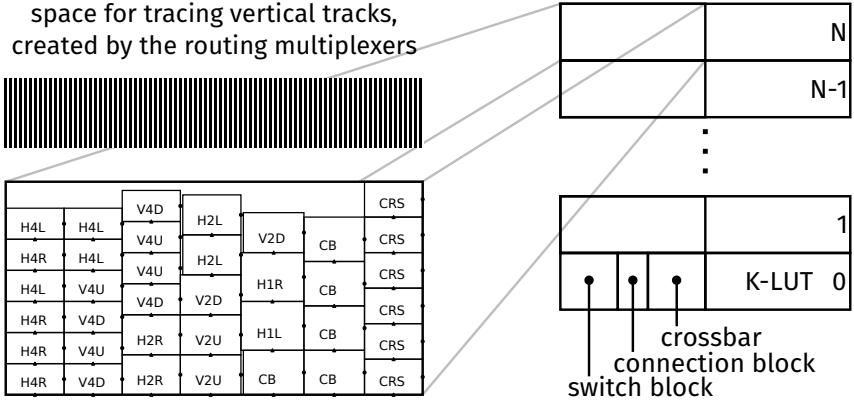
Khan and Ye, “An Evaluation on the Accuracy of the Minimum Width Transistor Area Models in Ranking the Actual Layout Area of FPGA”, FPL’16

Floorplan



Lewis et al., “Architectural enhancements in Stratix V”, FPGA’13

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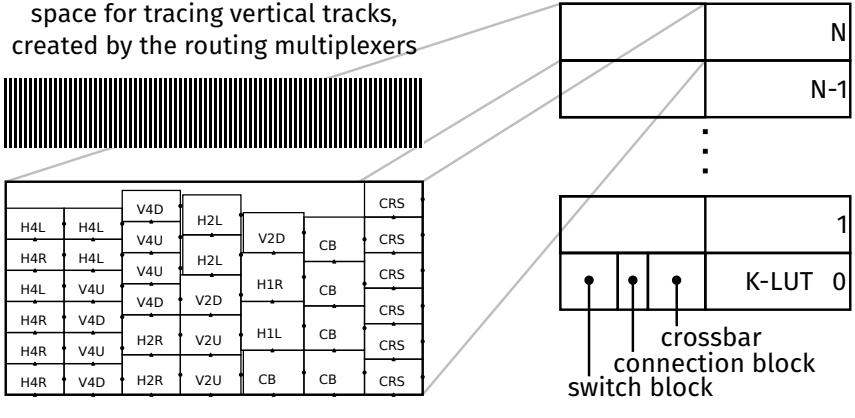

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Chromczak et al., “Architectural enhancements in Intel Agilex FPGAs”, FPGA’20

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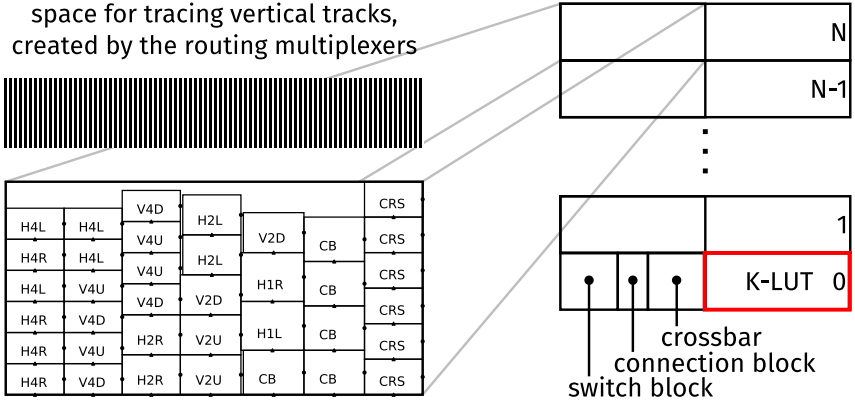

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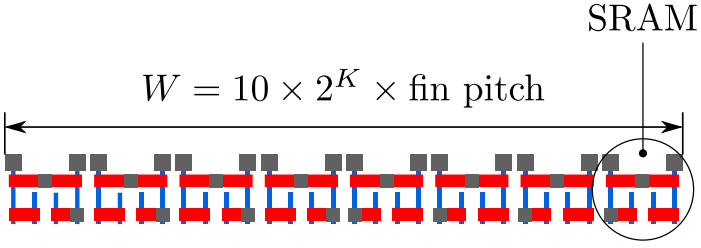
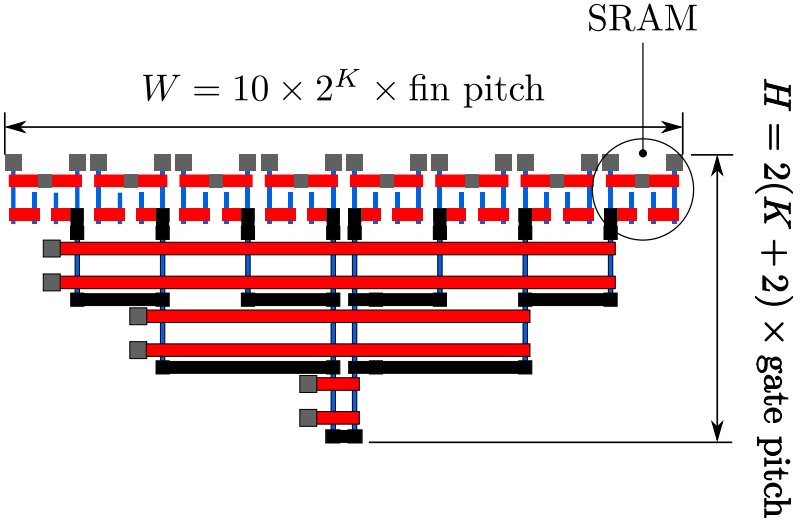
LUTs



Abusultan and Khatri, “A comparison of FinFET-based FPGA LUT designs”, GLSVLSI’14

LUTs



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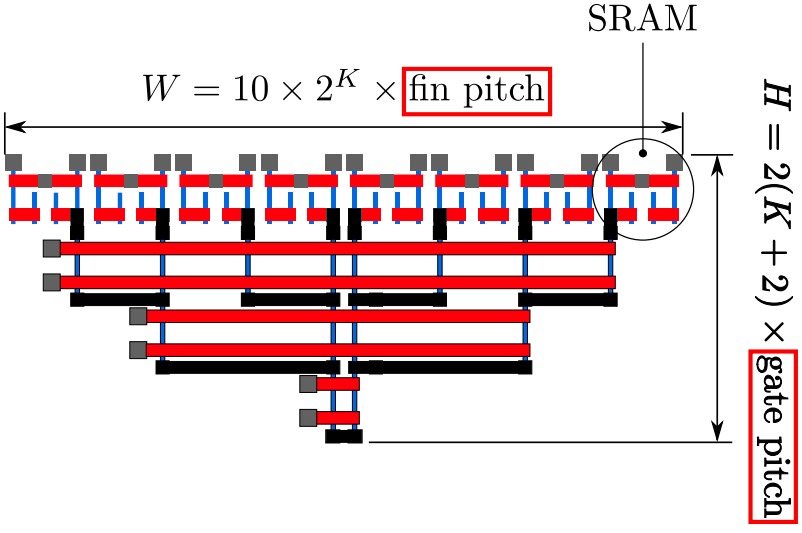

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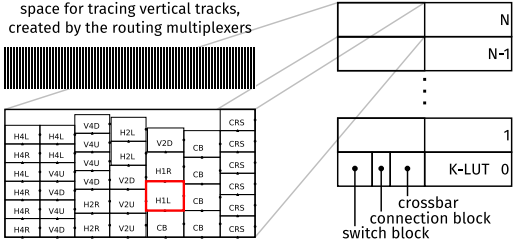
Multiplexers



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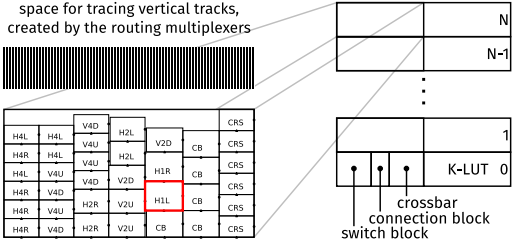

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  Chromczack et al., FPGA'20

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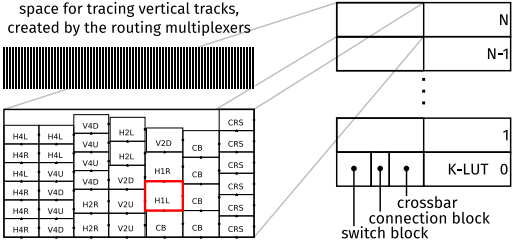

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  Chiasson, MSc Thesis, University of Toronto, 2013

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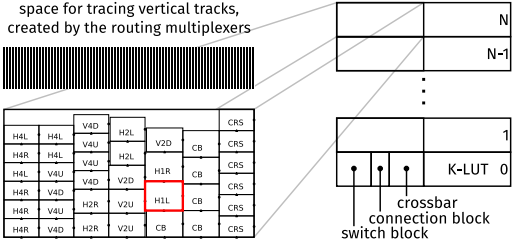

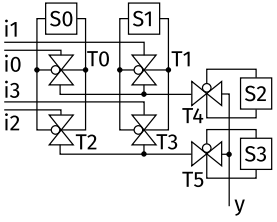

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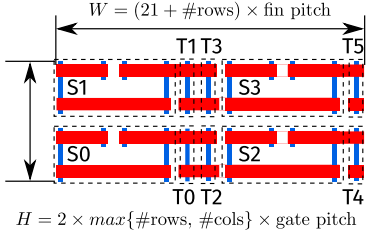
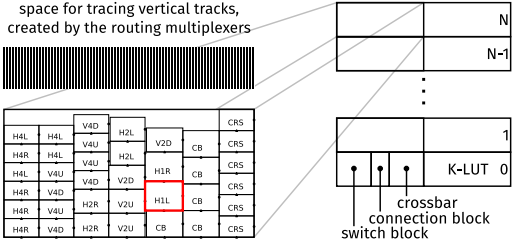
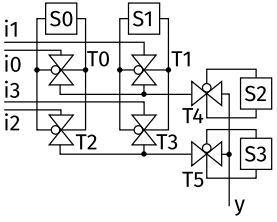
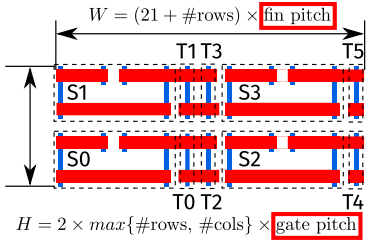


Multiplexers



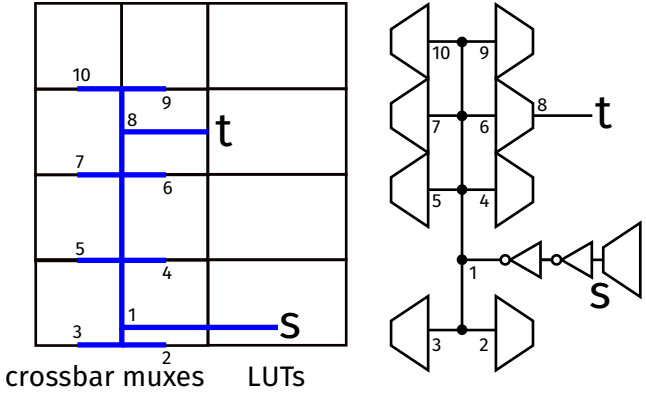


- All muxes transmission-gate-based
  Chromczack et al., FPGA'20
- All transmission-gates of minimum drive-strength (1 fin)
  Chiasson, MSc Thesis, University of Toronto, 2013

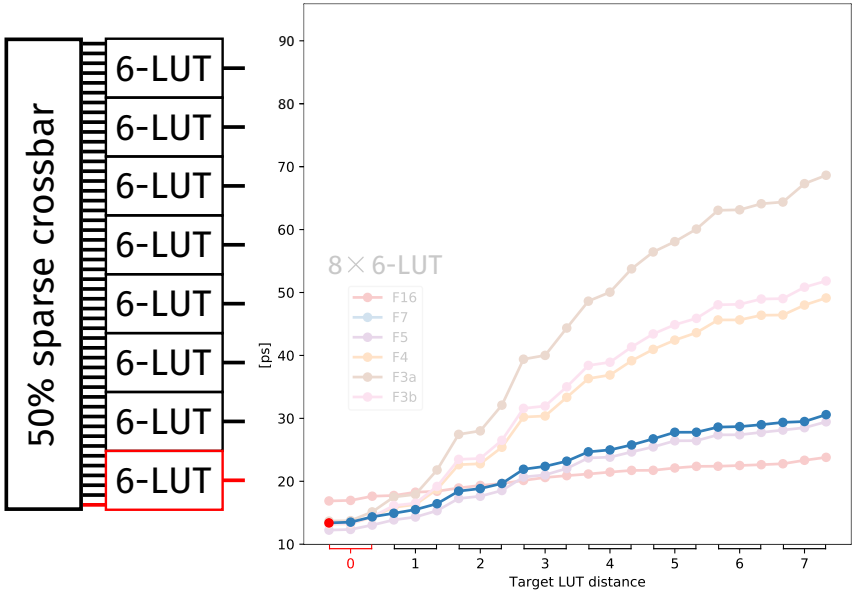


Delay Measurement

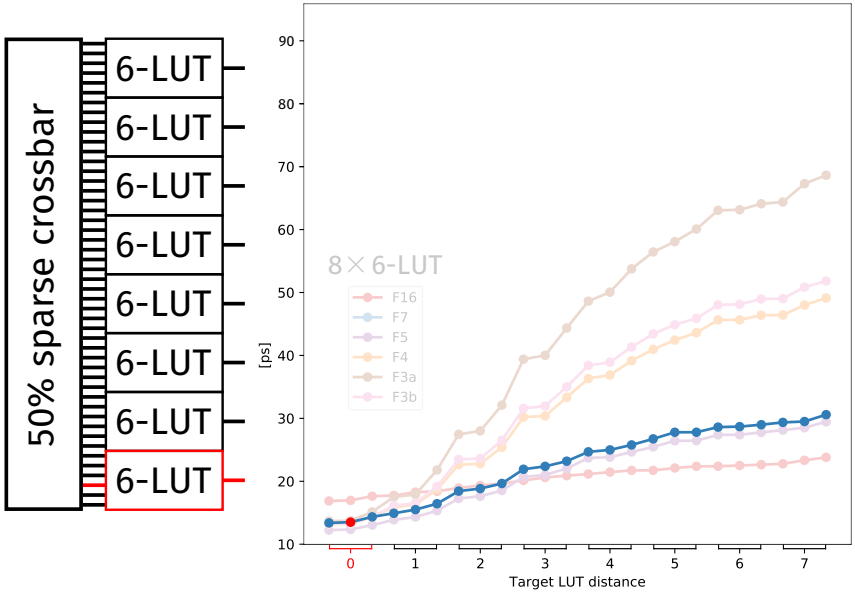
Local Connections



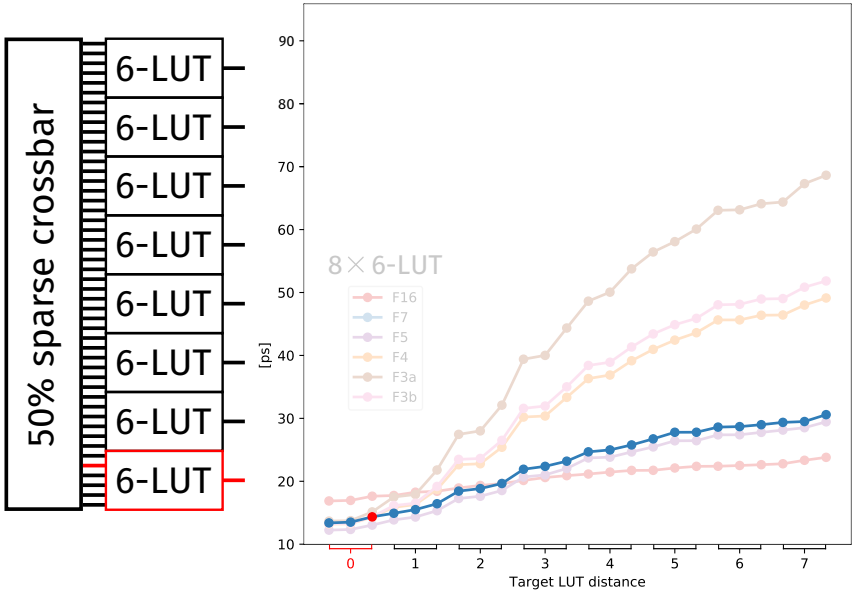
Local Connections: Cluster Feedback Delays



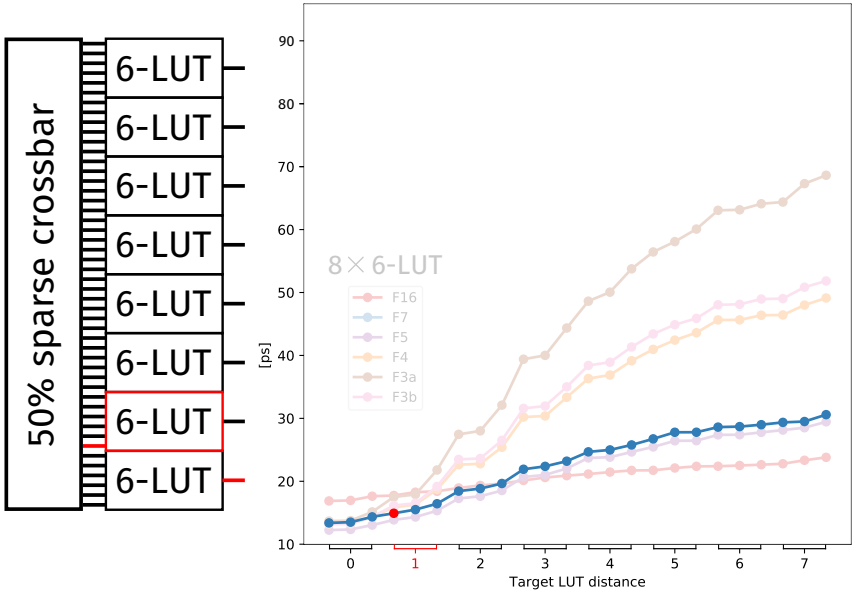
Local Connections: Cluster Feedback Delays



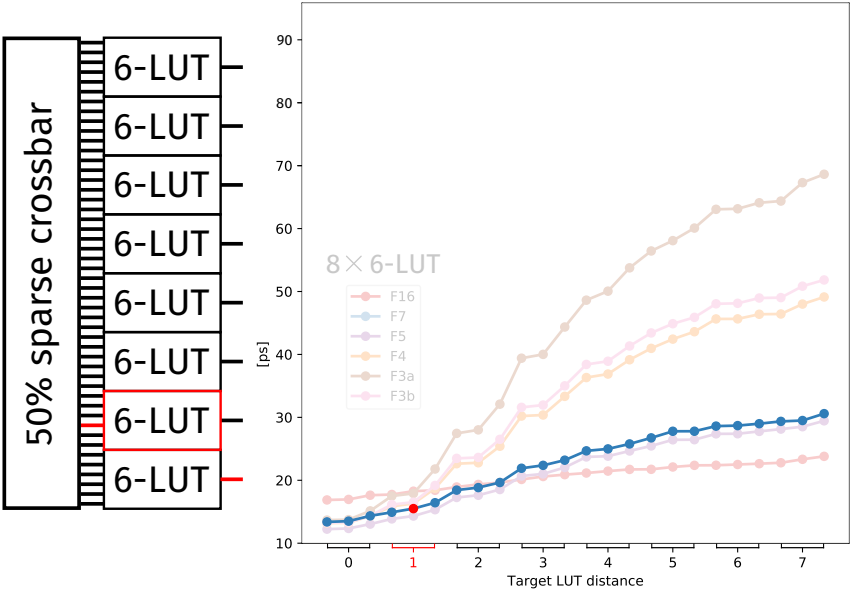
Local Connections: Cluster Feedback Delays



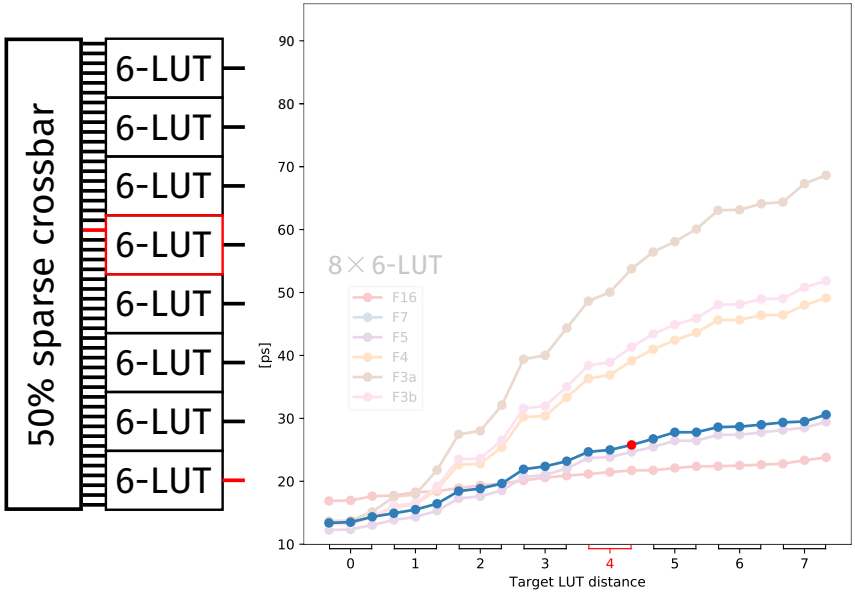
Local Connections: Cluster Feedback Delays



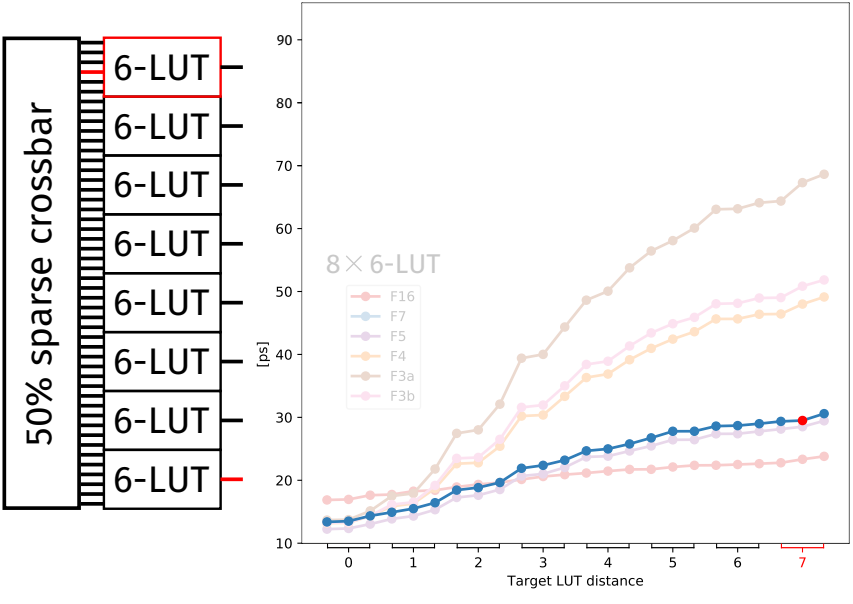
Local Connections: Cluster Feedback Delays



Local Connections: Cluster Feedback Delays

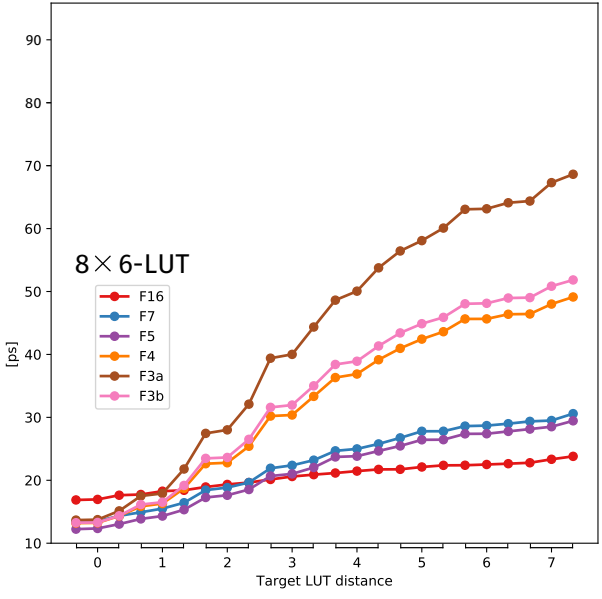


Local Connections: Cluster Feedback Delays



Local Connections: Cluster Feedback Delays

	pitch [nm]	R' [Ω/μm]
F16	64	31.6
F7	40	128.7
F5	38	151.6
F4	26	392.9
F3a	22	666.4
F3b	22	396.7



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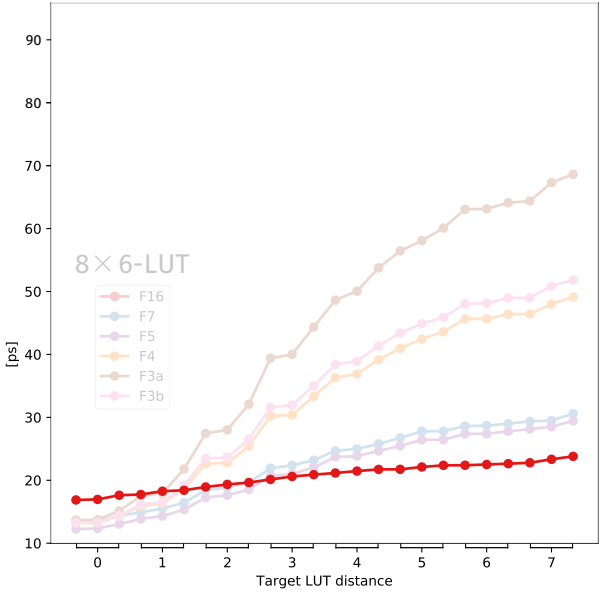

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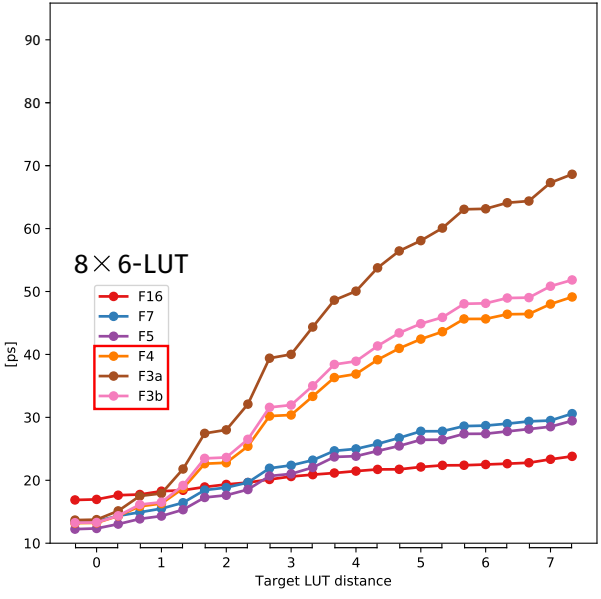

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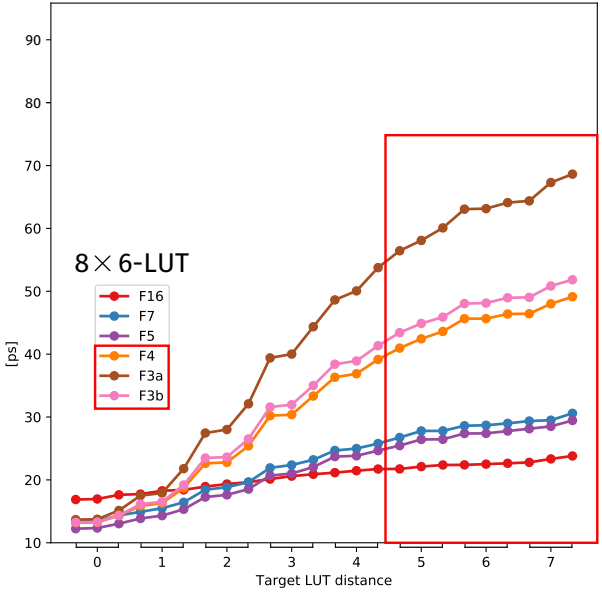

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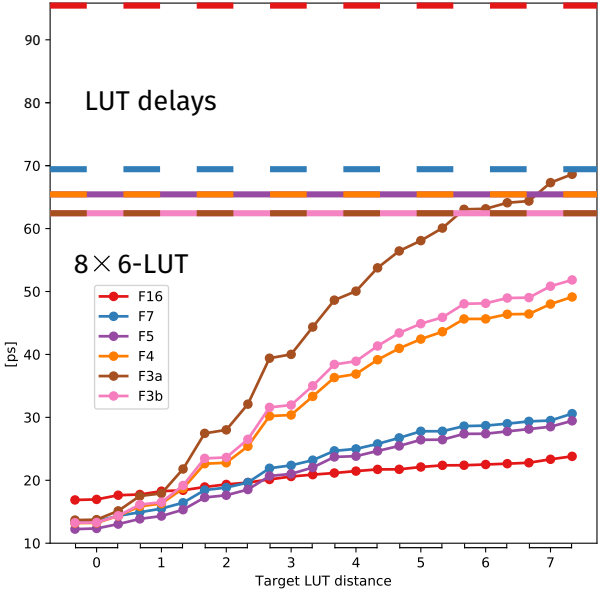

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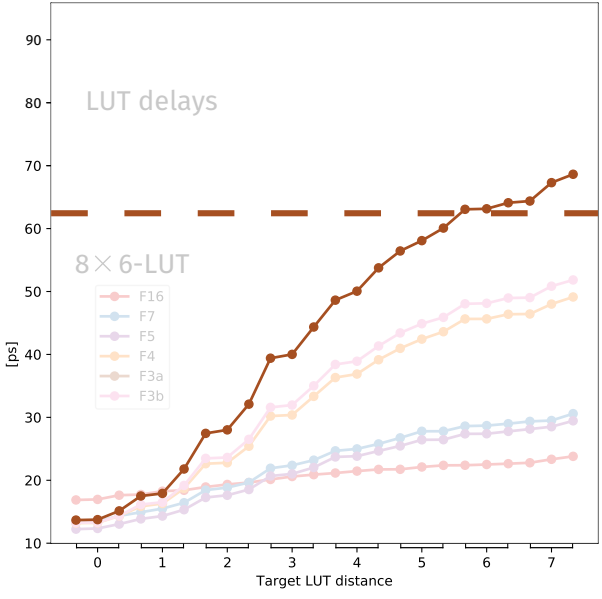
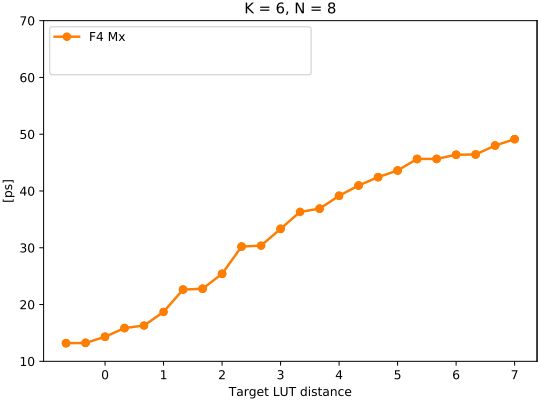
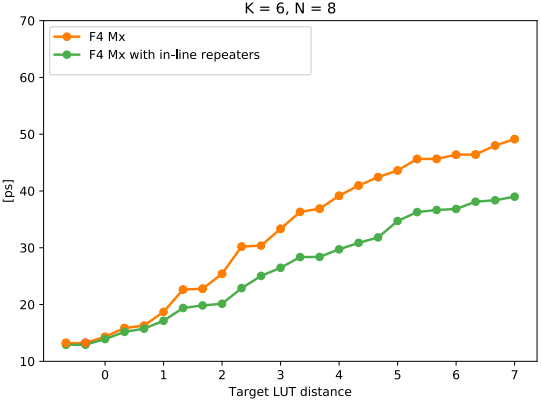
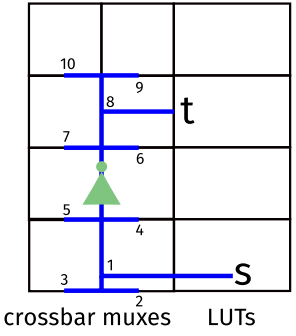


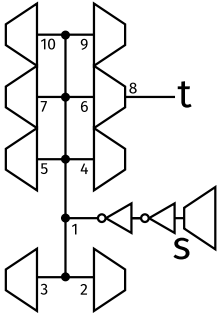
Local Connections: Cluster Feedback Delays



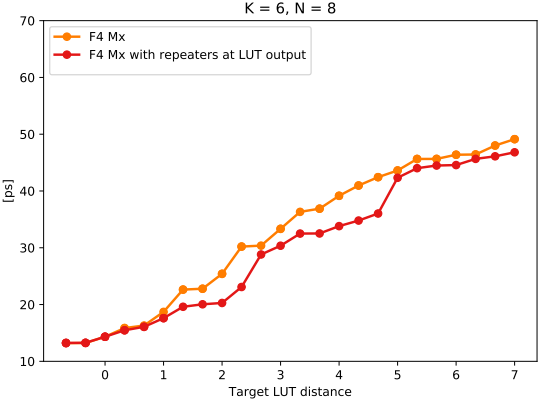
Local Connections: Cluster Feedback Delays

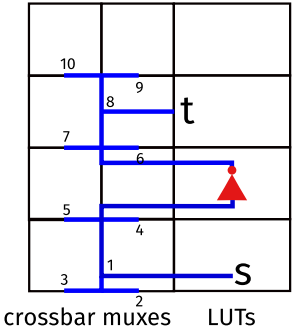


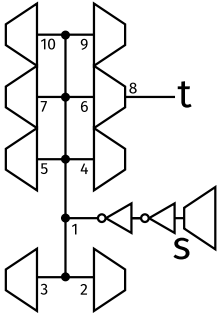




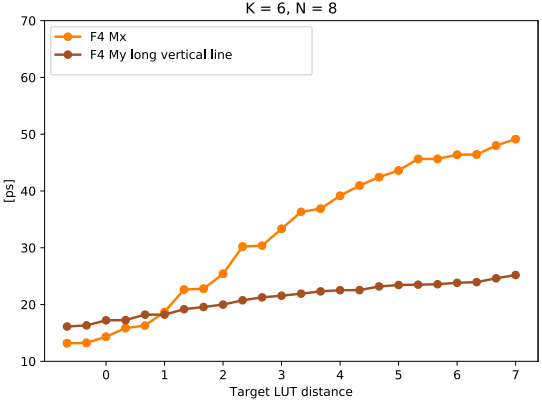
Local Connections: Cluster Feedback Delays

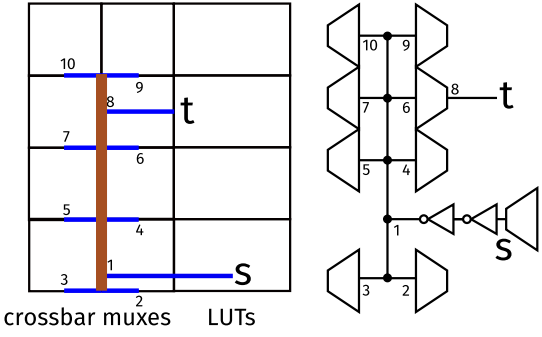




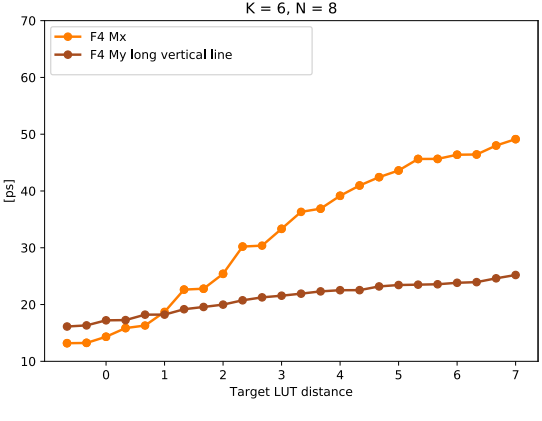


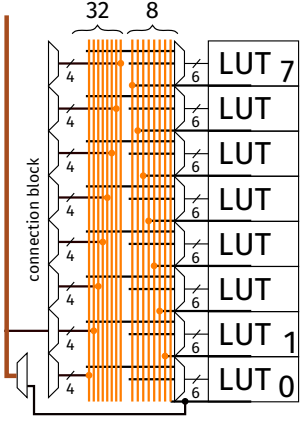
Local Connections: Cluster Feedback Delays





Thick Local Connections: Thick Metal is Scarce





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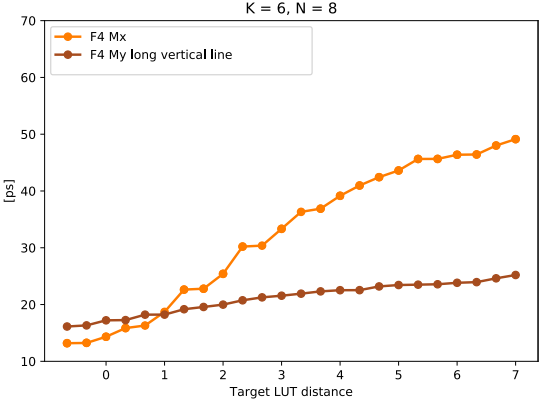

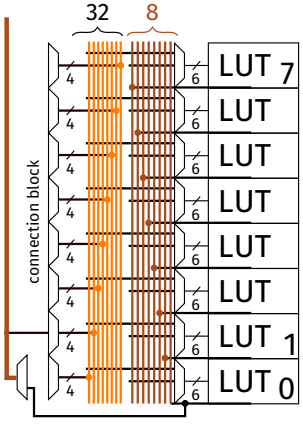

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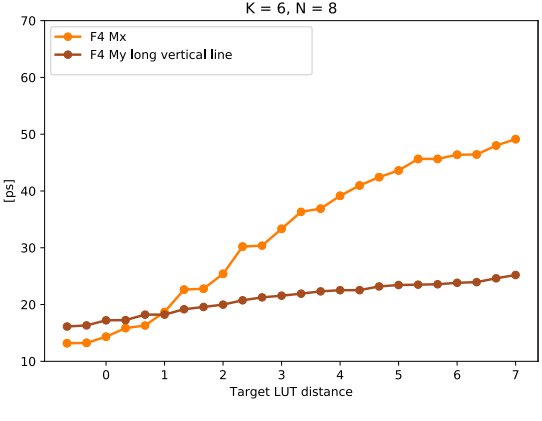

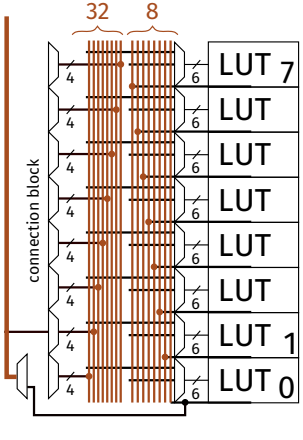

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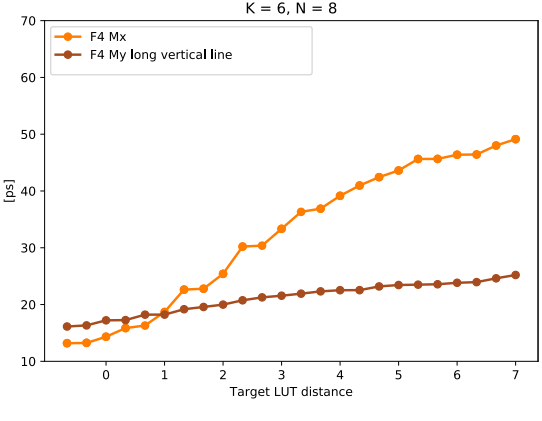

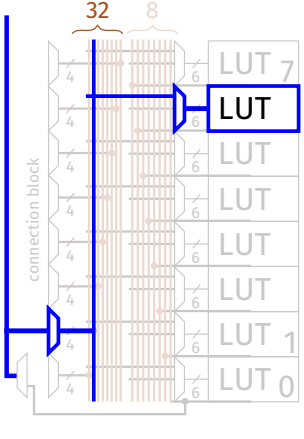

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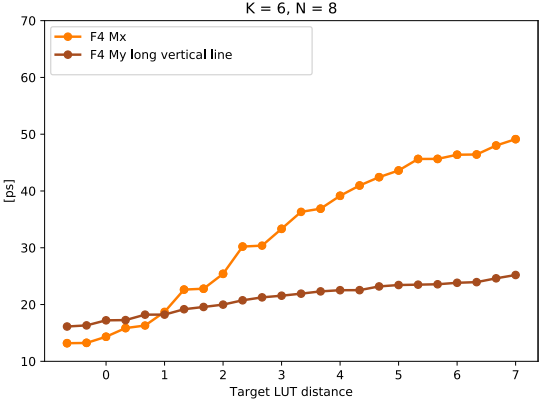

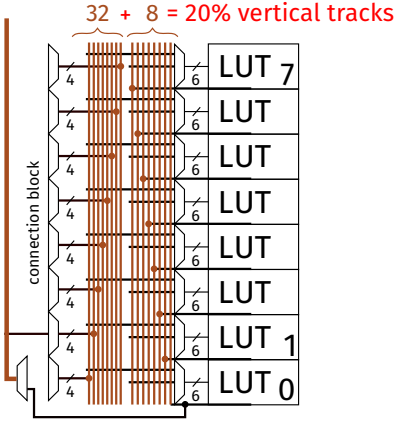

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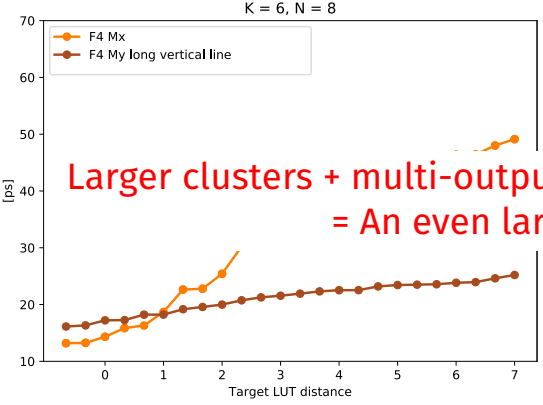
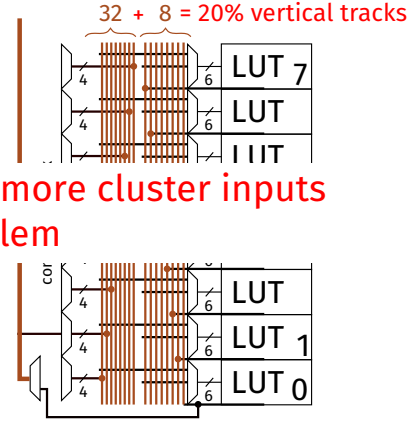
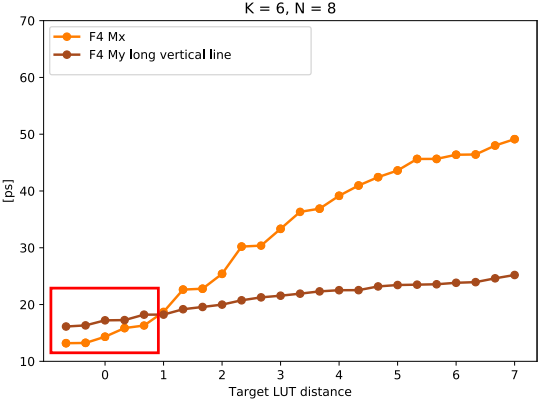


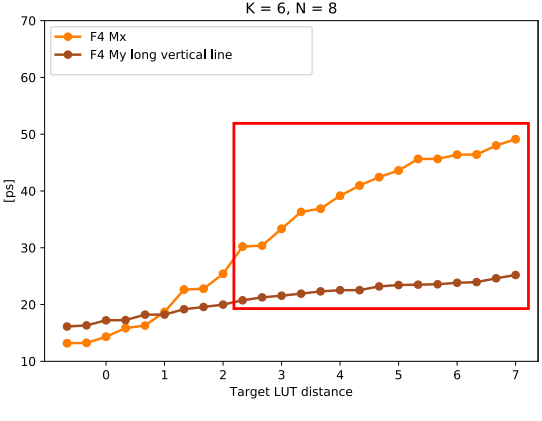


Larger clusters + multi-output LUTs + more cluster inputs
= An even larger problem

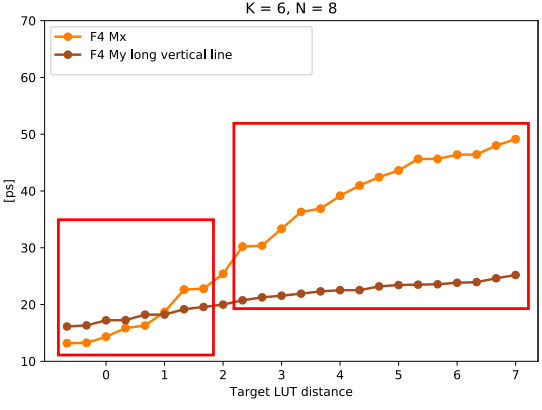
Thick Local Connections: Small Clusters to the Rescue

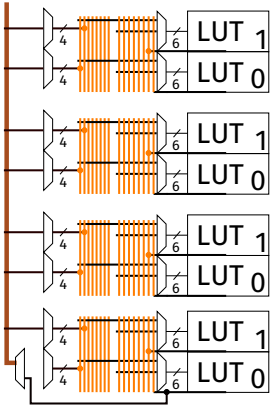


Thick Local Connections: Small Clusters to the Rescue



Thick Local Connections: Small Clusters to the Rescue





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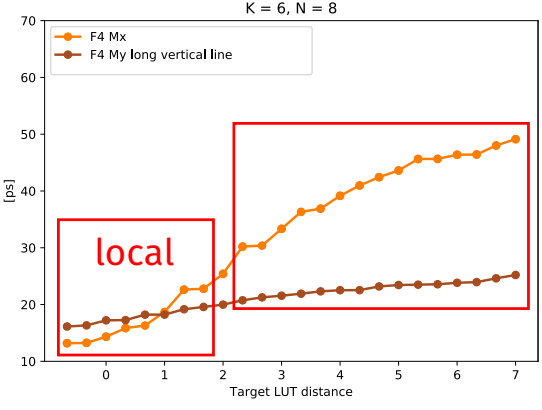

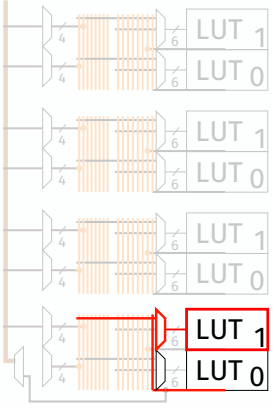

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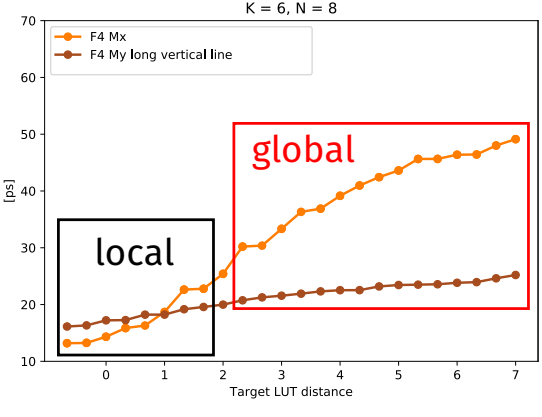
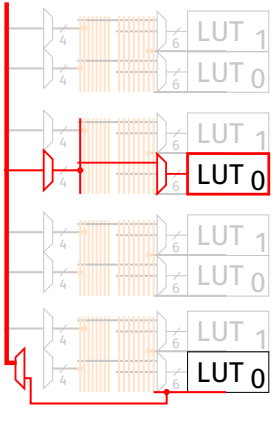
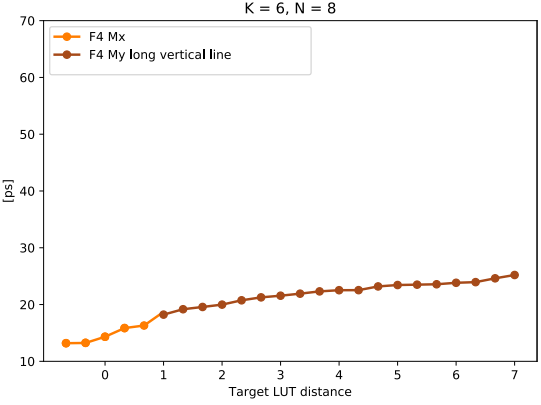




Thick Local Connections: Small Clusters to the Rescue



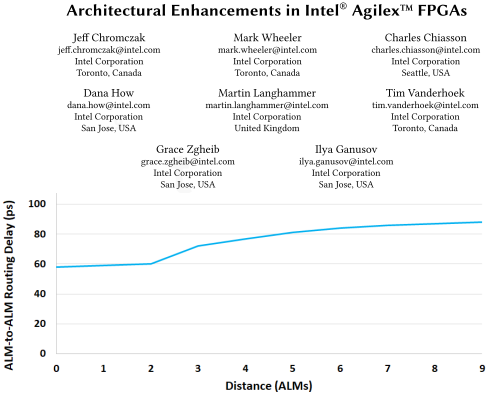
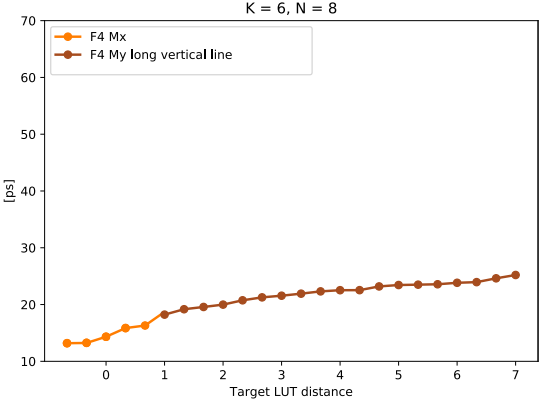
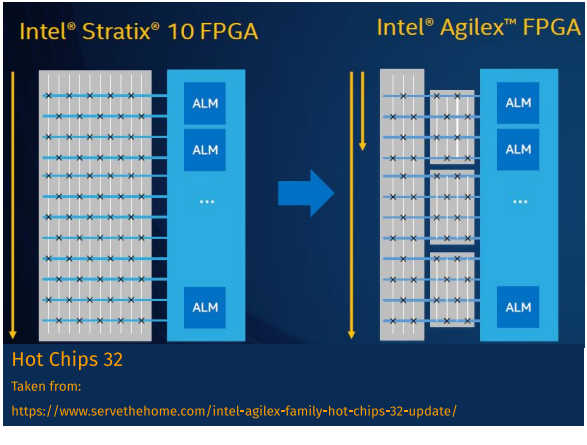


Figure 9: ALM-to-ALM routing delay improvement

Thick Local Connections: Small Clusters to the Rescue





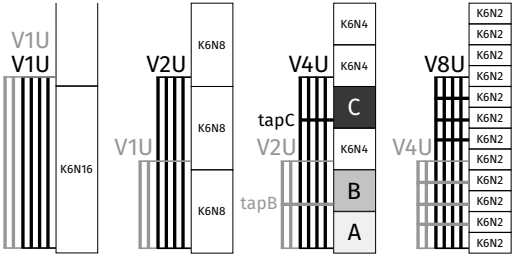
Exploring Cluster Sizes across Technology Nodes

Experimental Setup

- Clusters of 2, 4, 8, and 16 6-LUTs

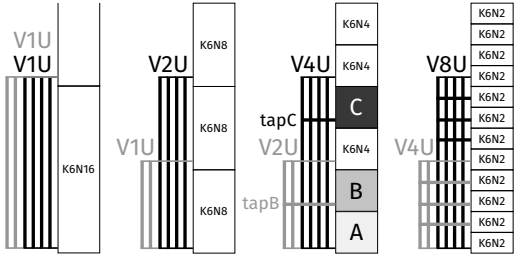
Experimental Setup

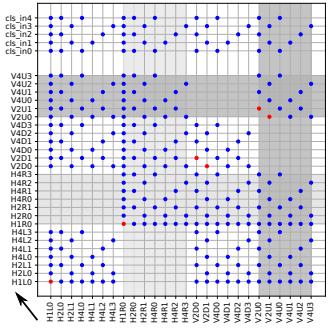
- Clusters of 2, 4, 8, and 16 6-LUTs
- Channel composition exploration



Experimental Setup

- Clusters of 2, 4, 8, and 16 6-LUTs
- Channel composition exploration
- Switch-patterns tailored for high-resistance lower metal





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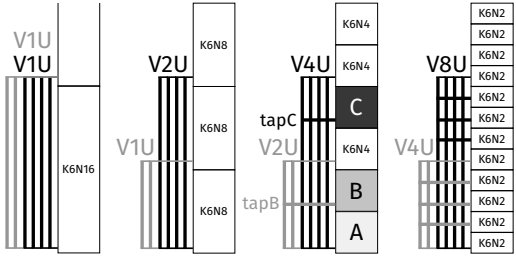
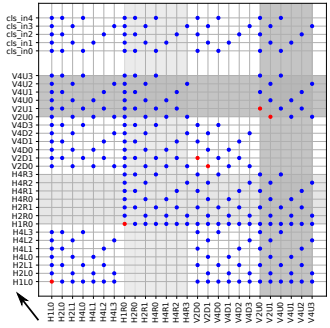
- Clusters of 2, 4, 8, and 16 6-LUTs
- Channel composition exploration
- Switch-patterns tailored for high-resistance lower metal
- MCNC benchmarks + VTR8.0

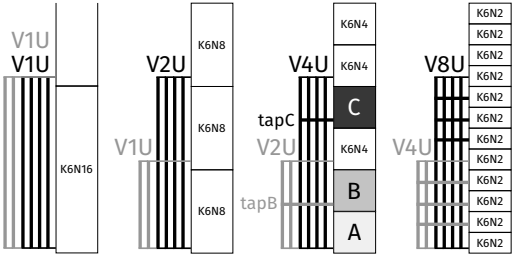


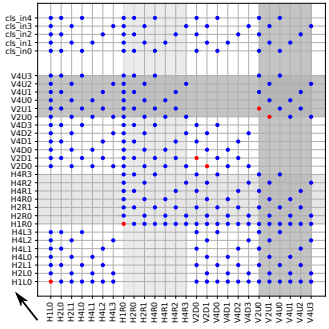


Experimental Setup

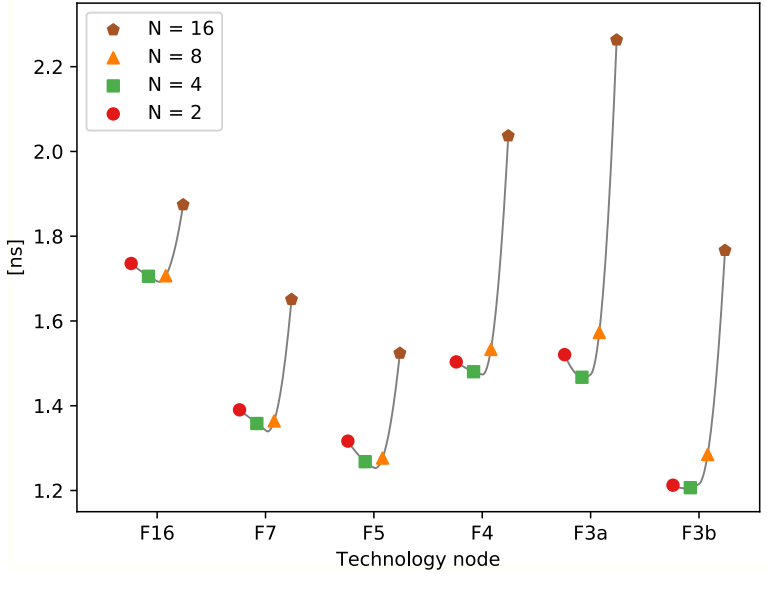
- Clusters of 2, 4, 8, and 16 6-LUTs
- Channel composition exploration
- Switch-patterns tailored for high-resistance lower metal
- MCNC benchmarks + VTR8.0

(Details in the paper)

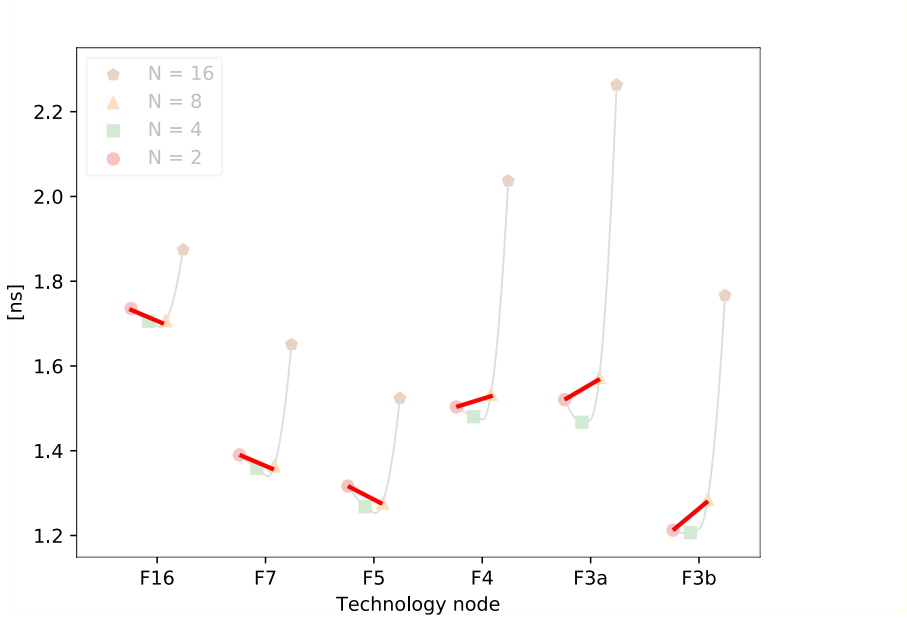




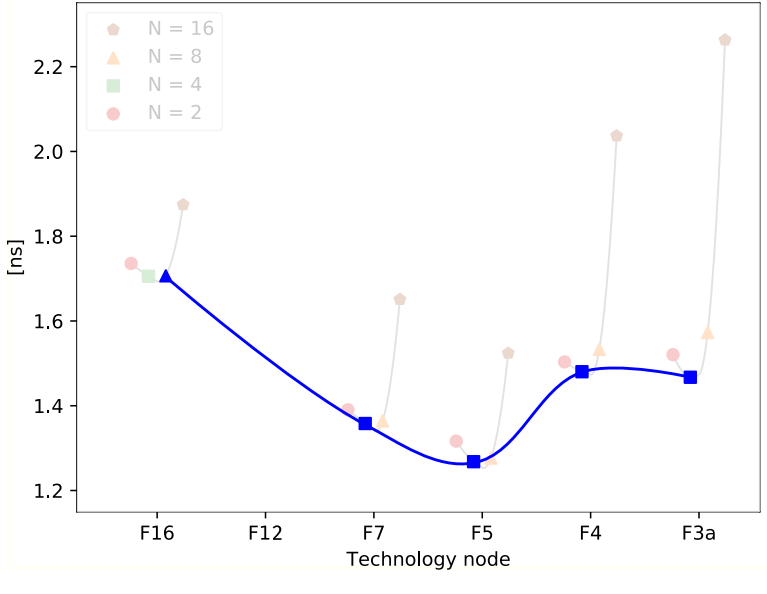
Cluster Sizes: Routed Delay Results



Cluster Sizes: Routed Delay Results



Performance Scaling



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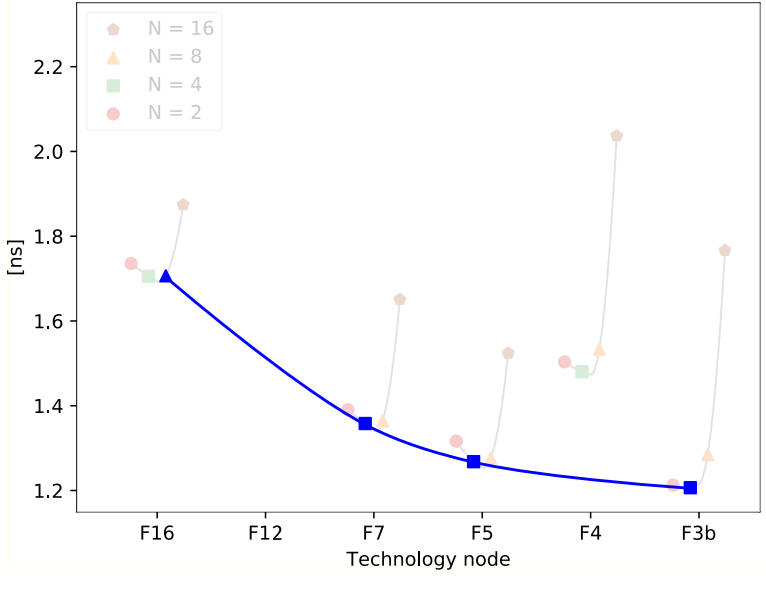
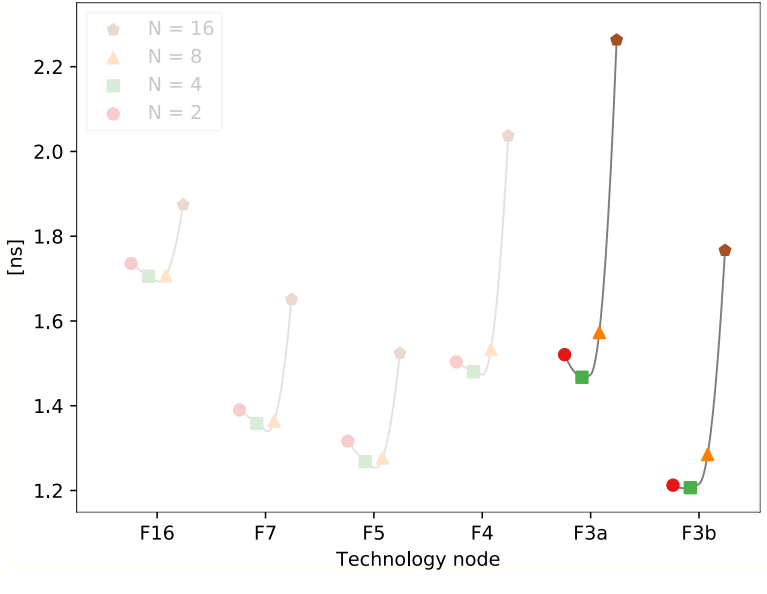


Performance Scaling



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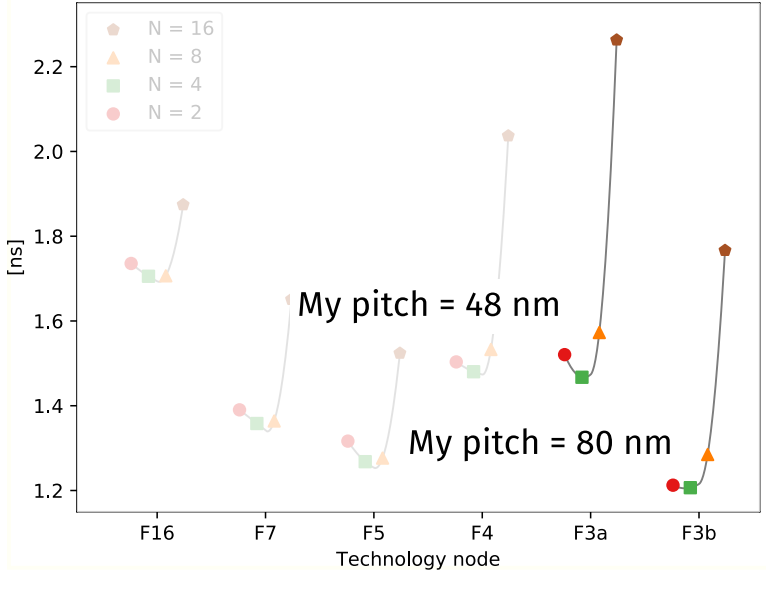
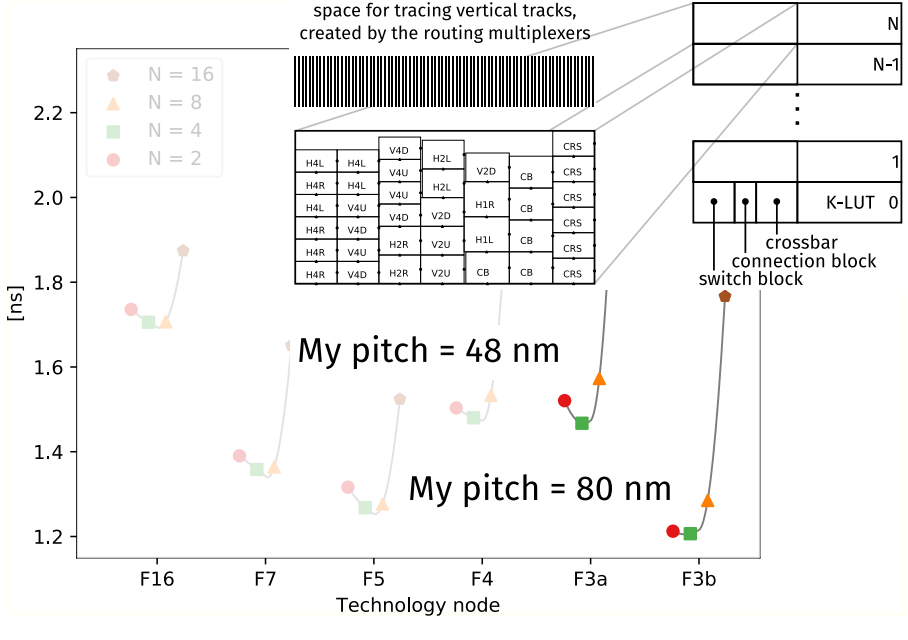


Performance Scaling



Performance Scaling

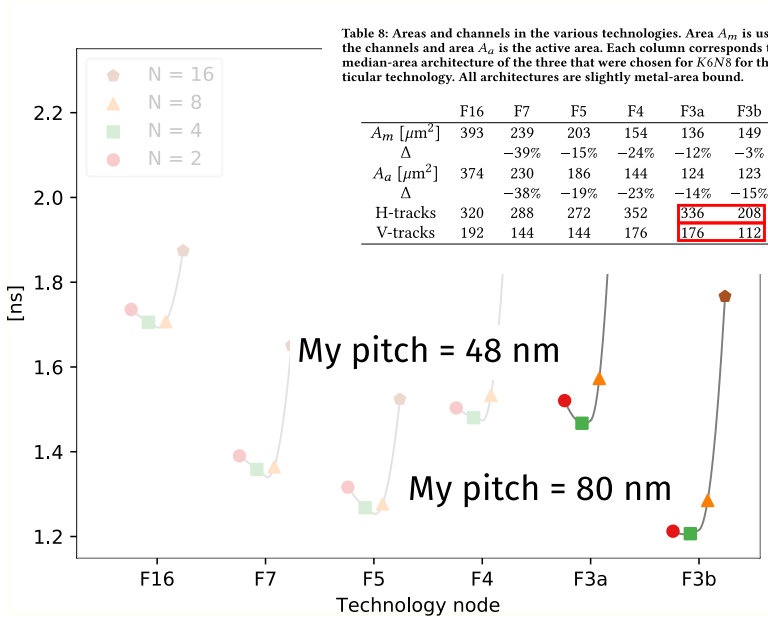


Table 8: Areas and channels in the various technologies. Area A_m is used by the channels and area A_a is the active area. Each column corresponds to the median-area architecture of the three that were chosen for $K6N8$ for the particular technology. All architectures are slightly metal-area bound.

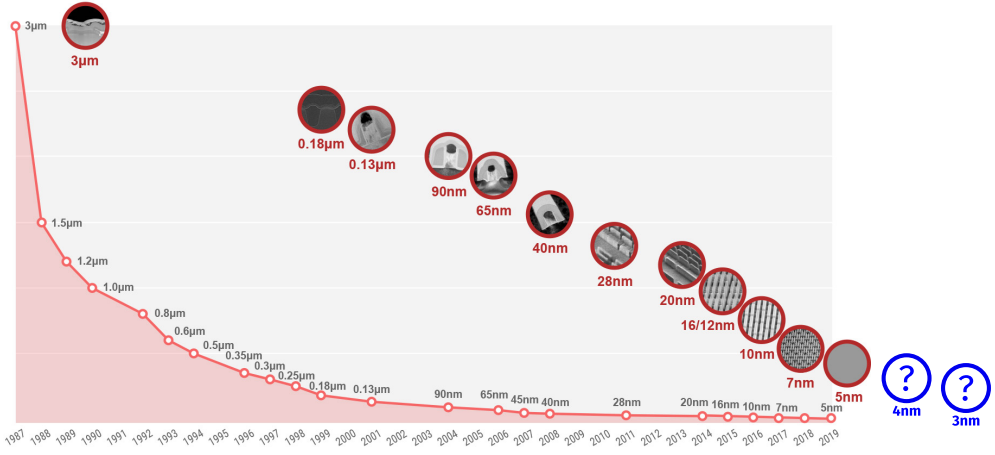
	F16	F7	F5	F4	F3a	F3b
A_m [μm^2]	393	239	203	154	136	149
Δ		−39%	−15%	−24%	−12%	−3%
A_a [μm^2]	374	230	186	144	124	123
Δ		−38%	−19%	−23%	−14%	−15%
H-tracks	320	288	272	352	336	208
V-tracks	192	144	144	176	176	112

-38%

-36%

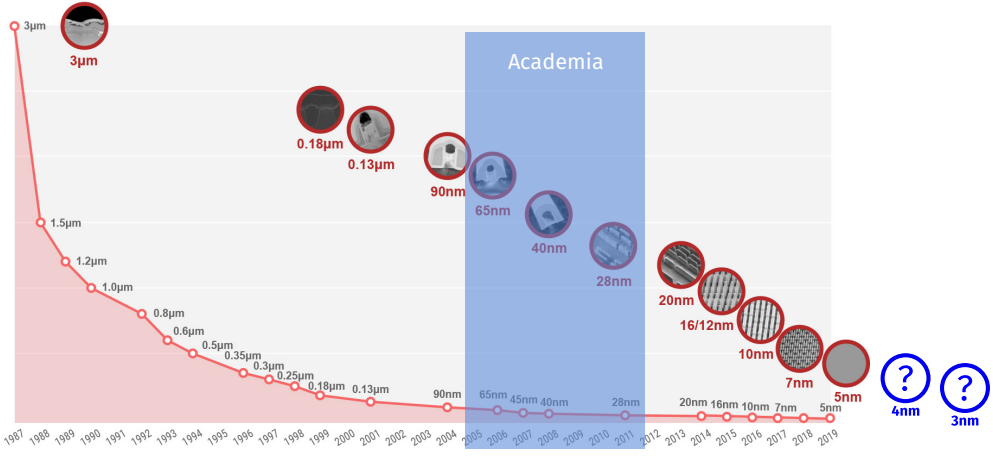
Summary

Summary



Source: TSMC (https://www.tsmc.com/english/dedicatedFoundry/technology/logic)

Summary



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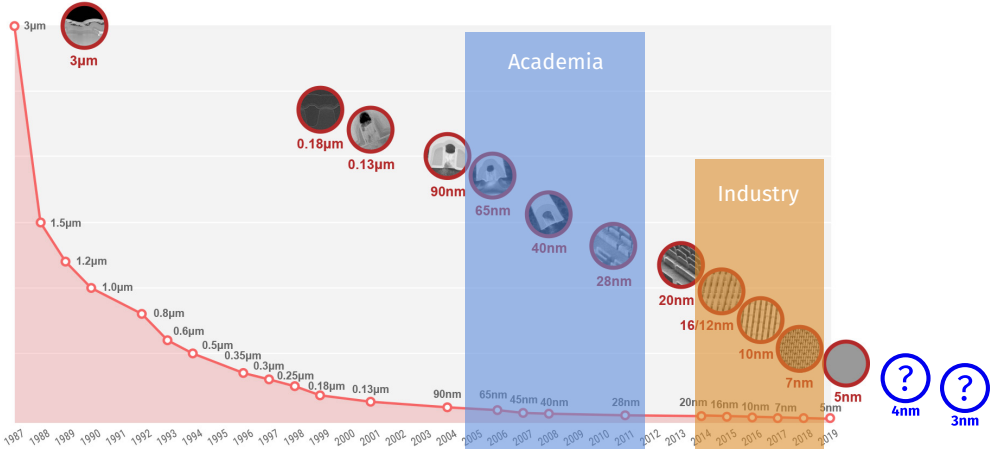
Summary



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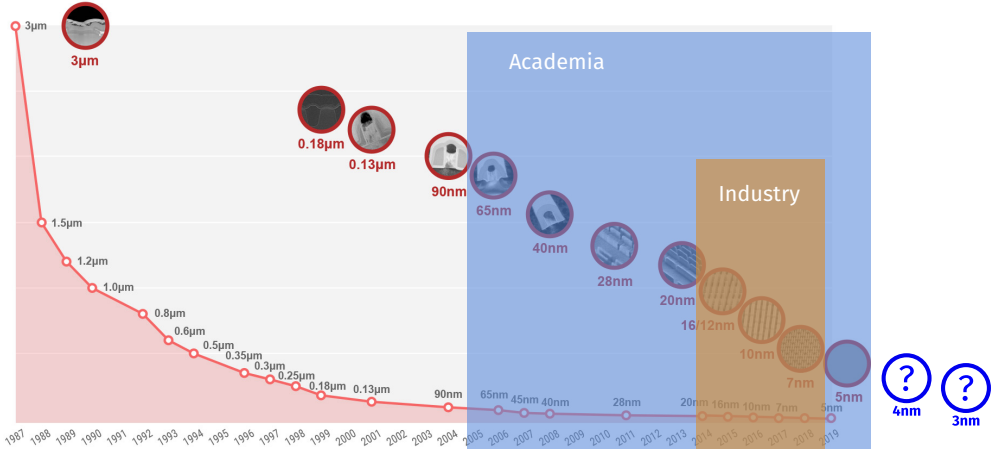
Summary



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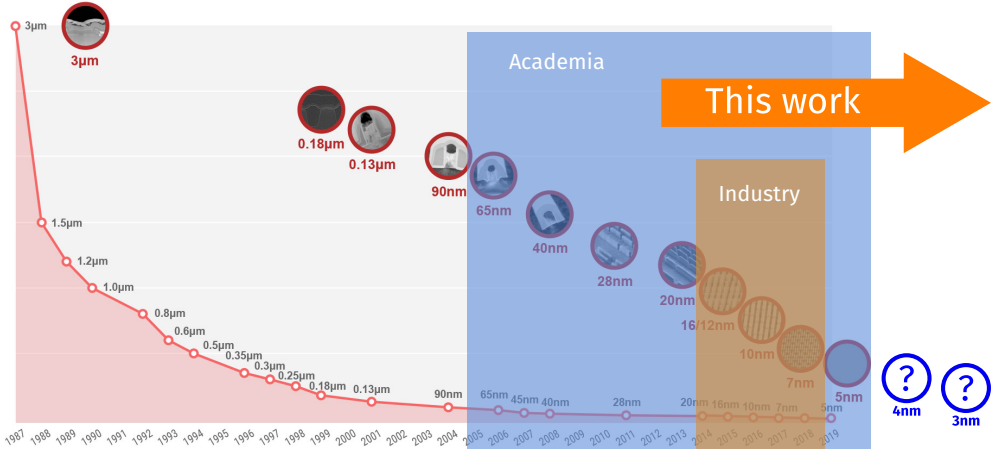
Summary



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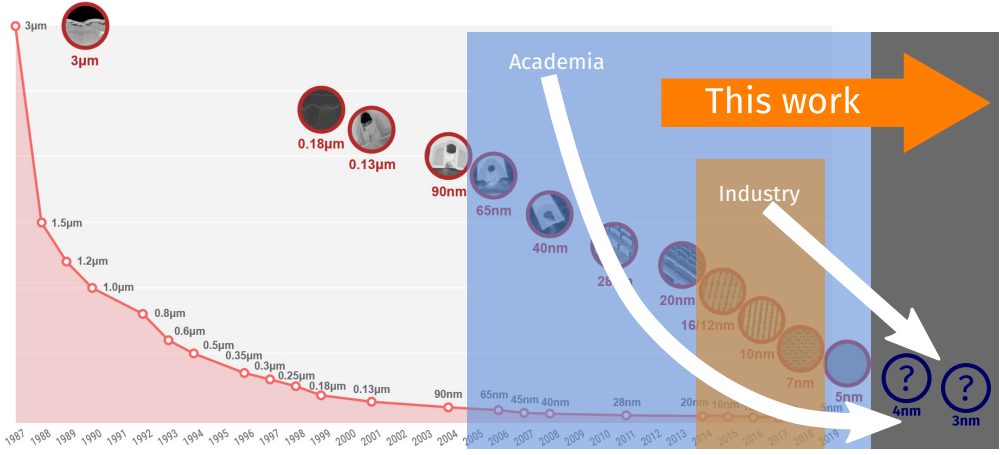
Summary



Source: TSMC (https://www.tsmc.com/english/dedicatedFoundry/technology/logic)

Thank you for attention

https://github.com/EPFL-LAP/fpga21-scaled-tech